


Article

Selective Harmonic Elimination in a Wide Modulation Range Using Modified Newton–Raphson and Pattern Generation Methods for a Multilevel Inverter

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Received: 19 January 2018; Accepted: 11 February 2018; Published: 22 February 2018

Abstract: Considering the aim of having low switching losses, especially in medium-voltage and high-power converters, the pre-programmed pulse width modulation technique is very useful because the generated harmonic content can be known in advance and optimized. Among the different low switching frequency techniques, the Selective Harmonics Elimination (SHE) modulation method is most suitable because of its direct control over the harmonic spectrum. This paper proposes a method for obtaining multiple solutions for selectively eliminating specific harmonics in a wide range of modulation indices by using modified Newton–Raphson (NR) and pattern generation techniques. The different pattern generation and synthesis approach provide more degrees of freedom and a way to operate the converter in a wide range of modulation. The modified Newton–Raphson technique is not complex and ensures fast convergence on a solution. Moreover, multiple solutions are obtained by keeping a very small increase in the modulation index. In the previous methods, solutions were not obtainable at all modulation indices. In this paper, only exact solutions to the low-order harmonics elimination for Cascaded H-bridge inverter are reported for all modulation indices. Analytical and simulation results prove the robustness and correctness of the technique proposed in this paper.

Keywords: Modified Newton–Raphson(M-NR); selective harmonics elimination; multi-level inverter; pulse width modulation; transcendental equations; modulation index

1. Introduction

The performance of a VSC mostly depends on the type of PWM strategy chosen for its operation. The PWM schemes for power converters can be broadly classified as high switching frequency PWM, such as sine PWM; space vector PWM; and low switching frequency, such as Selective Harmonics Elimination (SHE), Space Vector Modulation (SVM), and selective harmonics mitigations (SHM) schemes [1–10]. The high switching frequency PWM schemes (in kHz) are used in applications where power quality is of more importance than switching losses (mainly low power applications). Whereas low switching frequency (50–800 Hz) [11,12]. PWM schemes are employed in medium-voltage, high-power voltage source converters, where switching losses are the main constraint, along with power quality. Among the different low switching frequency techniques, SHE is a pre-programmed modulation method that was proposed to eliminate two lower-order harmonics by having additional

switching angles in the square wave voltage waveform [13]. It was developed into a generalized means of obtaining the desired voltage by selectively eliminating the lower-order harmonics [14]. The SHE PWM exhibits some distinct features in comparison to other PWM techniques such as: (i) low converter switching frequency, which contributes to the reduction in switching losses and hence increases the efficiency and reliability of the converter; (ii) in SHE-PWM, unlike other PWM techniques, overmodulation is possible, which causes an increased utilization of the DC bus; (iii) selective elimination of lower-order harmonics results in high power quality and lower harmonic losses; (iv) high quality of output voltage and current also reduces the ripple in the DC link current and, therefore, a reduction in the size of the DC link filter components can be achieved.

Multilevel converters represent a very important topic in modern power electronics and many research groups are working on topologies, modulation techniques, and control algorithm strategies to improve the global behaviour of the system. In medium- and high-power applications, it is not good practice to use high switching frequencies because the thermal losses could damage the switching devices. Therefore, low switching frequency modulation techniques based on pre-computed PWM switching patterns can be very useful. The medium-voltage inverter operated with SHE normally has a quarter wave symmetrical stepped voltage waveform at output at fundamental frequency. However, several switches can be done in one quarter of the cycle to obtain a better quality output waveform as it will eliminate harmonics but at the cost of higher switching losses. The biggest challenge in the implementation of the SHE-PWM technique is solving the set of trigonometric equations with the multiplicity of angles obtained after applying a Fourier series analysis of the output waveforms. These sets of equations are highly non-linear and transcendental in nature and may exhibit multiple solutions, a unique solution, or no solution in a different range of modulation index. The methods most commonly used to solve these equations are numerical methods, algebraic methods, and evolutionary-algorithm-based optimization methods. The numerical methods include the conventional Newton–Raphson (NR) algorithm [14] and sequential homotopy [15]. The algebraic methods introduced recently include resultant elimination theory [16,17] and Groebner bases with symmetric polynomials [18]. The evolutionary-algorithm-based optimization methods include random searching methods that optimize an objective function based on a genetic algorithm [19], modified species-based particle swarm optimization [20,21], the ant-colony-based algorithm [22], artificial neural network real-time angle generation [23], the colonial competitive algorithm [24], and the bee algorithm [25]. A universal method based on equal area criteria also introduced in [26] tries to solve the problem by having only four equations, irrespective of number of voltage levels. In numerical techniques, for fast and sure convergence, a good initial guess is necessary and finding multiple solutions is difficult and involves complicated calculations. Metaheuristic-based optimization methods may not converge on an exact solution of the equations but rather minimize an objective function and give an approximate solution with a particular initial guess. The solution to this method is highly dependent on the formulation of the objective function and search space. Also, the solution depends on the parameter assumed in the algorithm and requires expert programming for getting reliable solutions. The limitations of numerical and metaheuristic methods can be overcome by algebraic methods that can provide all the solutions at a particular modulation index. However, because of the involvement of a high degree of polynomials, it is complicated and takes a lot of time to evaluate all possible solutions.

In this paper, a pattern synthesis approach based on different voltage levels at different modulation ranges is proposed and investigated. The trigonometric transcendental equations obtained from different patterns have been solved using a modified NR method. The proposed modified NR method is not sensitive to the initial guesses as in the case of the conventional NR method. Moreover, the modified NR method is also capable of generating multiple solutions in a modulation range, which is not possible with conventional NR methods. Different patterns have been synthesized for an 11-level cascaded H-bridge; three-phase inverter and switching angles are computed in a wide range of modulation indices with multiple solutions. In the existing literature, the problem is aggravated when the modulation index is low and generally few solutions are obtained. This limitation is overcome

in the proposed approach, which provides more flexibility and degrees of freedom and at least one solution for the entire range of the modulation index.

2. Eleven-Level Cascaded H-Bridge Inverter

The cascaded H-bridge multilevel inverter can have several H-bridge cells connected in cascades to obtain higher voltage and power at output with fewer rating power switches [27–35]. It consists of several separate DC sources to produce a stepped waveform very close to the sinusoidal voltage waveform with lesser THD. Its modular structure and circuit flexibility makes it more suitable for medium-voltage and high-power applications. Further the modulation method can be extended for more number of phases (>3) by simply increasing the number of legs horizontally.

In this paper a three-phase balanced system has been considered, which is mostly used in medium-voltage, high-power applications in industry. Figure 1 shows a three-phase H-bridge inverter with five separate DC sources in each leg connected in a cascade. The number of levels in the output voltage is given by $2N + 1$, where N is the number of separate DC sources; since there are five separate DC sources here, it will be an 11-level inverter and its phase voltage is given by $V_{an} = (V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5})$. Each cell can generate three voltage levels of $+V_{dc}$, 0 and $-V_{dc}$ at its terminal depending upon the switching states of power switches. The switching states and corresponding output from a cell are shown in Table 1. The main objective of the SHE-PWM technique is to obtain a desired output waveform very close to sinusoid and eliminate some undesired harmonics (usually lower-order harmonics) from the variable output voltage in a wide range of operations. In all the cell switches, S_{X1} (where X denotes the respective voltage source) and S_{X4} operate together, while S_{X2} and S_{X3} operate simultaneously but in a complementary way. To avoid direct short circuiting in the cell, some dead band is also provided, which is normally in the range of microseconds.

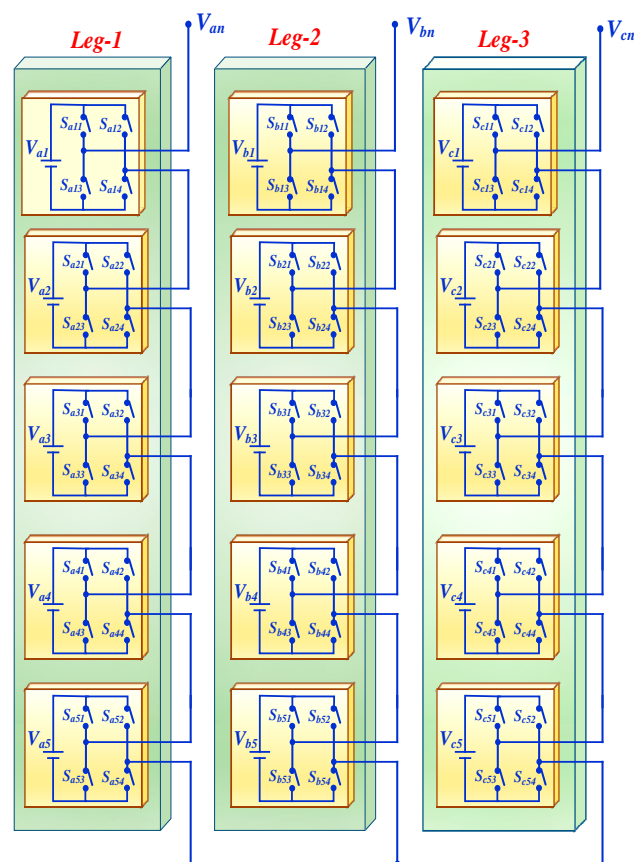


Figure 1. Eleven-level, three-phase cascaded H-bridge inverter.

Table 1. Switching angles in different quadrants.

Case	Switches' States	Cell Output Voltage
i.	(1,3) → 0 and (2,4) → 0	0
ii.	(1,3) → 0 and (2,4) → 1	$-V_{dc}$
iii.	(1,3) → 1 and (2,4) → 0	$+V_{dc}$
iv.	(1,3) → 1 and (2,4) → 1	0

3. Problem Formulation and Mathematical Modelling

The AC output voltage of the cascaded H-bridge is given by the sum of voltages from different H-bridges connected in cascades. To analyse the output voltage waveform from the inverter, the Fourier series expansion technique is used. The general Fourier series expansion can be expressed as:

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t), \quad (1)$$

where Fourier coefficients are given by:

$$\left. \begin{aligned} a_0 &= \frac{1}{T} \int_0^T f(t) dt \\ b_n &= \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt \\ b_n &= \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt \end{aligned} \right\}. \quad (2)$$

The general L-level inverter output voltage waveform was generated in the fundamental frequency switching scheme from the multilevel inverter by considering equal separate DC voltage. After applying the Fourier series theory to the output voltage waveform of a multilevel inverter, which has the odd quarter-wave symmetry shown in Figure 2, $a_0 = 0$ and $a_n = 0$. Also, because of even wave symmetry, all even-numbered terms in b_n coefficients will be zero. The third harmonics need not be considered for elimination because the triple harmonics automatically get cancelled in the line-to-line voltages for a balanced three-phase system and will not appear in final output waveforms. The Fourier series coefficients are obtained as in Equation (3):

$$b_n = \begin{cases} \frac{4E}{n\pi} \sum_{k=1}^N \cos(n\alpha_k), & \text{for odd } n \\ 0, & \text{for even } n \end{cases}, \quad (3)$$

where b_n is the amplitude of the n th harmonics and N is the number of separate DC sources or maximum attainable level in the output waveform. Therefore, the phase to neutral output voltage can be expressed as:

$$V_{out} = \sum_{n=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^N \cos(n\alpha_k) \right] \sin(n\omega t). \quad (4)$$

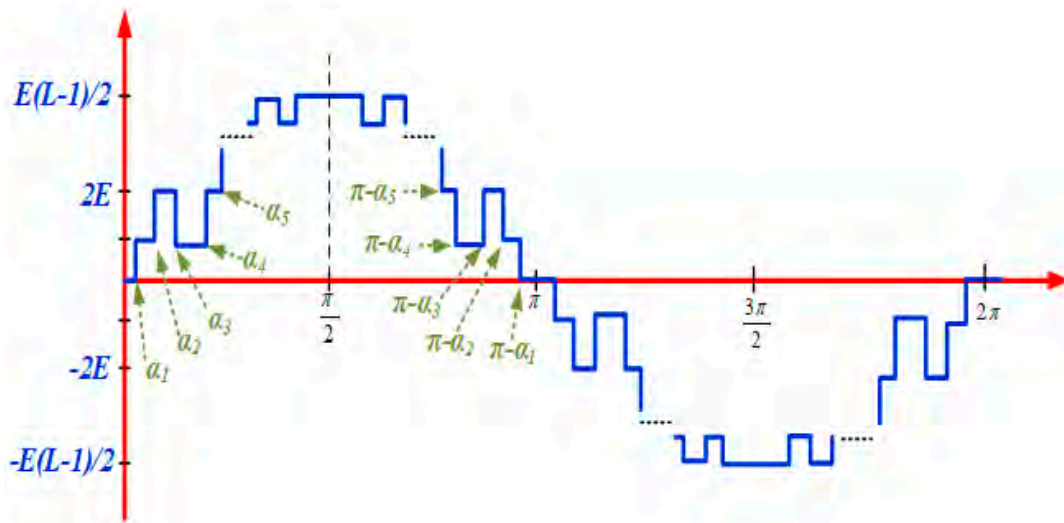


Figure 2. Generalized quarter wave symmetrical L-level output voltage waveform.

In a more general form, the output voltage can be written as:

$$V_{out} = \sum_{n=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^N \pm \cos(n\alpha_k) \right] \sin(n\omega t). \tag{5}$$

For the rising edge of α_k , the sign will be “+” and for the falling edge of α_k it will be “-”. Thus, the equation for the fundamental frequency switching control method can be expressed as:

$$V(\omega t) = \sum_{n=1,3,5\dots}^{\infty} \frac{4E}{n\pi} (\pm \cos(n\alpha_1) \pm \cos(n\alpha_2) \pm \dots \pm \cos(n\alpha_N)) \sin(n\omega t). \tag{6}$$

Considering only rise edges, Equation (6) can be developed as follows:

$$\left. \begin{aligned} \sum_{k=1}^N \cos \alpha_k - M &= 0 \\ \sum_{k=1}^N \cos(5\alpha_k) &= 0 \\ \dots \\ \sum_{k=1}^N \cos(n\alpha_k) &= 0 \end{aligned} \right\} \tag{7}$$

$$M = \frac{V_1}{V_{1max}} = \frac{V_1}{4NE/\pi} = \frac{m}{N} \tag{8}$$

or the SHE equation can be formulated as

$$\begin{aligned} &\text{minimize } f(\alpha) \\ &\text{subject to} \\ &g_k(\alpha) \leq 0, k = 1, 2, \dots, M \quad . \\ &h_t(\alpha) = 0, t = 1, 2, \dots, T \\ &L^i \leq \alpha^i \leq U^i, i = 1, 2, \dots, N \end{aligned} \tag{9}$$

The feasible range of solutions in mathematical notation can be represented by

$$\Omega = \left\{ \alpha = [\alpha^1, \alpha^2, \alpha^3, \dots, \alpha^N] \in R^N \mid g_k(\alpha) \leq 0, h_t(\alpha) = 0, L^i \leq \alpha^i \leq U^i \forall i \right\}. \quad (10)$$

Here the first four non-triple lower harmonics, i.e., 5th, 7th, 11th and 13th, are reconsidered for elimination and the required fundamental voltage magnitude at the output is achieved. For linear operation of the converter, the modulation index M should be $0 < M < 1$. For a cascaded multilevel inverter operated at fundamental frequency with five separate DC sources, a total, $2^5 = 32$ different switching patterns are possible. Out of a total of 32 patterns, 16 are just a mirror image of the horizontal axis and only nine patterns are useful for generating physically correct waveforms, as shown in Figure 3.

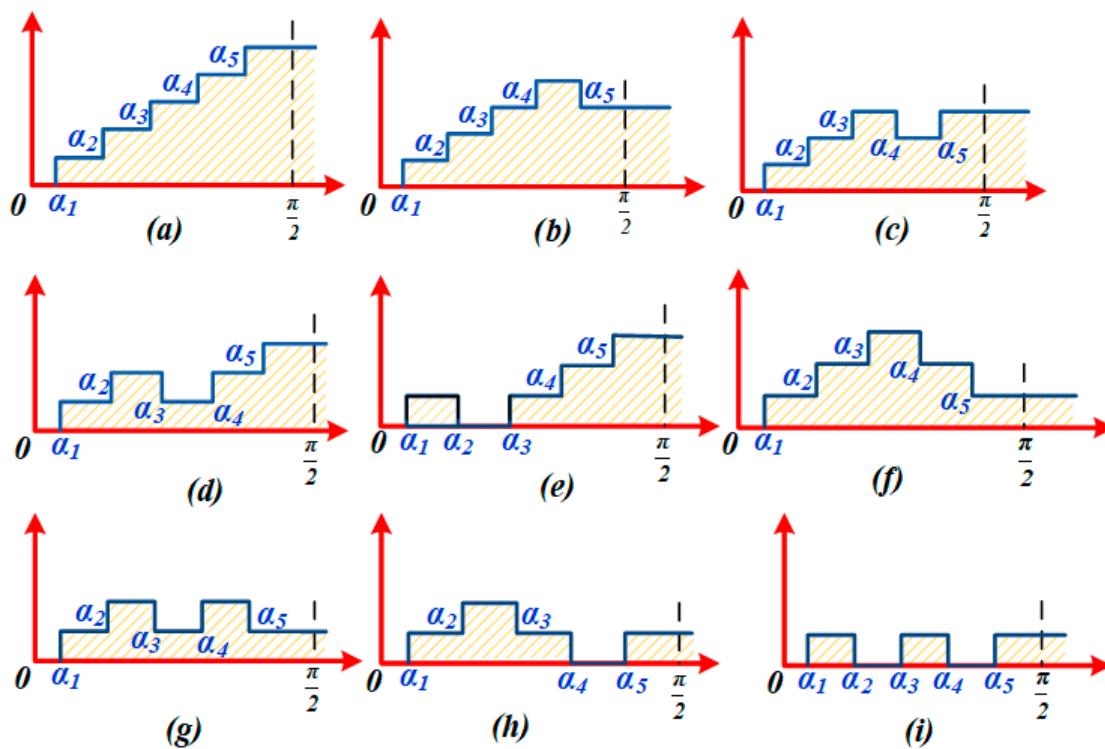


Figure 3. Different pattern synthesis switching transitions from the 11-level cascaded H-bridge inverter.

- (a) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$; (b) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\uparrow}, \alpha_{5\downarrow}$; (c) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\downarrow}, \alpha_{5\uparrow}$; (d) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\downarrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$;
 (e) $\alpha_{1\uparrow}, \alpha_{2\downarrow}, \alpha_{3\uparrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$; (f) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\downarrow}, \alpha_{5\downarrow}$; (g) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\downarrow}, \alpha_{4\uparrow}, \alpha_{5\downarrow}$; (h) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\downarrow}, \alpha_{4\downarrow}, \alpha_{5\uparrow}$;
 (i) $\alpha_{1\uparrow}, \alpha_{2\downarrow}, \alpha_{3\uparrow}, \alpha_{4\downarrow}, \alpha_{5\uparrow}$.

4. Modified NR Algorithm to Solve the SHE Problem

The Modified NR method begins with any random initial guess in the range 0 to $(\pi/2)$ (assuming quarter wave odd symmetry in the PWM waveform) and generally converges at a zero of a given system of nonlinear equations. If there exists a solution, it usually runs for a large number of iterations. Here the algorithm is run in a discrete numbers of points, usually in very small steps of modulation index change (in this paper, modulation steps of 0.0001 are considered). The multiplicity of solutions in a particular range of modulation index is due to its convergence at different solution sets at different M in the neighbourhood. One can still decrease the step size to search for more solutions in some particular range of M . The flow chart is given in Figure 4.

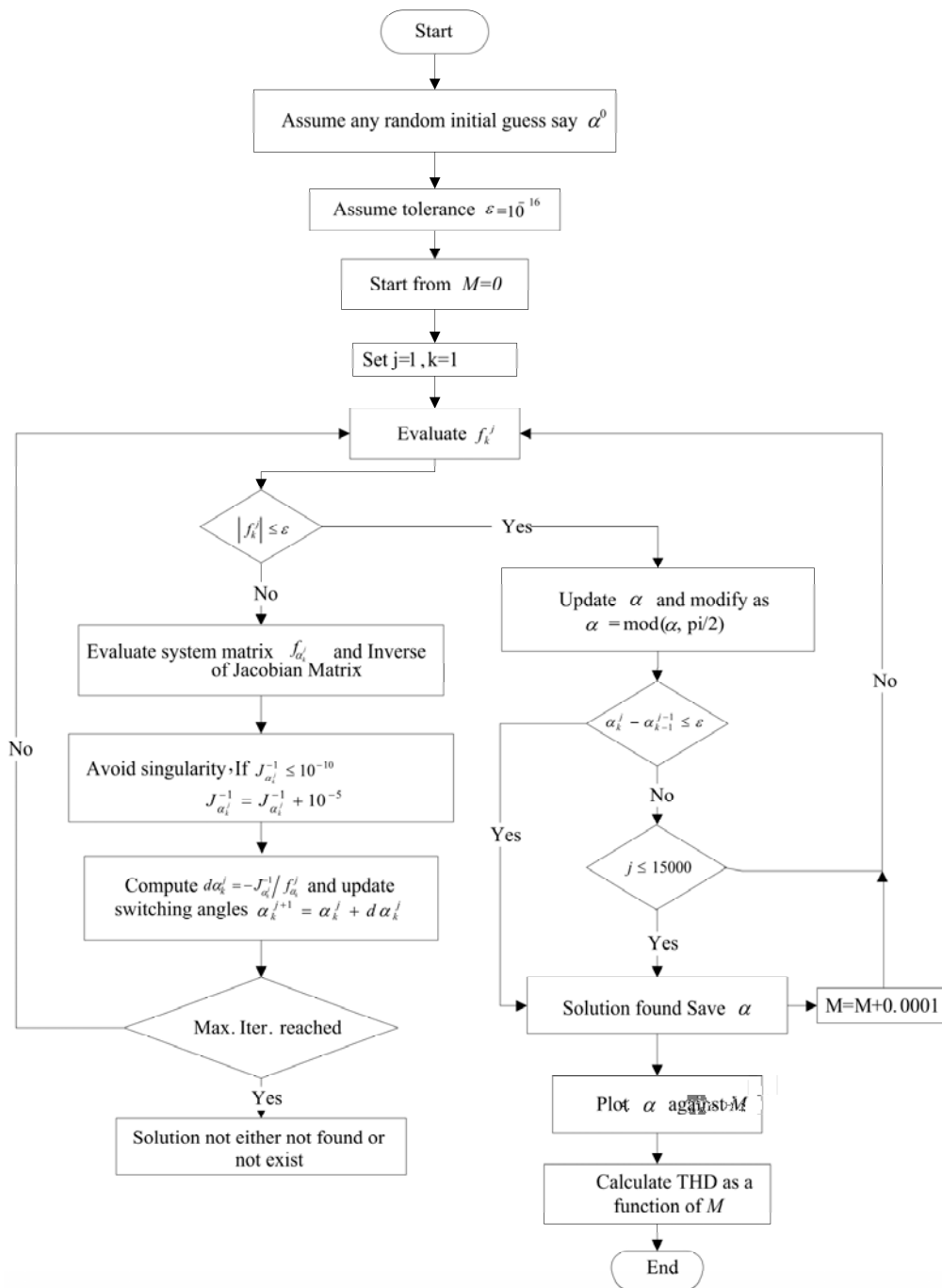


Figure 4. Flow chart of modified NR for solving SHE problem.

This is executed repetitively in the complete range of the modulation index, i.e., from 0 to 1, to find multiple solutions for PWM with guaranteed convergence. The algorithm ensures all possible solutions are generated, starting with a random initial guess. The THD for all solutions has been calculated at different modulation index using Equation (9); here harmonics of the order upto 200 are considered for the calculations:

$$\%THD = \sqrt{\left[\sum_{n=5,7,11,13,\dots}^{200} \left(\frac{V_n}{V_1} \right)^2 \right]} \times 100. \tag{11}$$

Mathematical equations for PWM output waveforms have been developed. The modified NR method discussed in Section 4 is applied to evaluate the switching instants for the bidirectional power switches. The technique presented in this work was first tested on the well-known results available in the literature—for instance, the five-angle case for a three-phase system eliminating non-triple, low-order harmonics—and the results obtained are compared. Some new switching angles were found by this method. For instance, at $M = 0.55$, for all rising edge cases, there were three sets of switching angles $\{34.46, 44.57, 54.24, 65.40, 78.04\}$, $\{19.75, 39.10, 56.52, 63.57, 88.20\}$, and $\{4.05, 37.30, 41.98, 79.31, 88.63\}$, for $\alpha_1, \alpha_2, \alpha_3, \alpha_4$, and α_5 . The third set obtained here is novel and may have better performance than the first two sets; in addition, it provides higher redundancy. It clearly reflects the robustness of the technique.

The selective solutions for the entire pattern shown in Figure 3 have been evaluated using the modified NR method and the results are shown for the different patterns in Figure 5. The switching instants for a particular pattern are obtained at output in the modulation range of 0 to 1 (in steps of 0.0001).

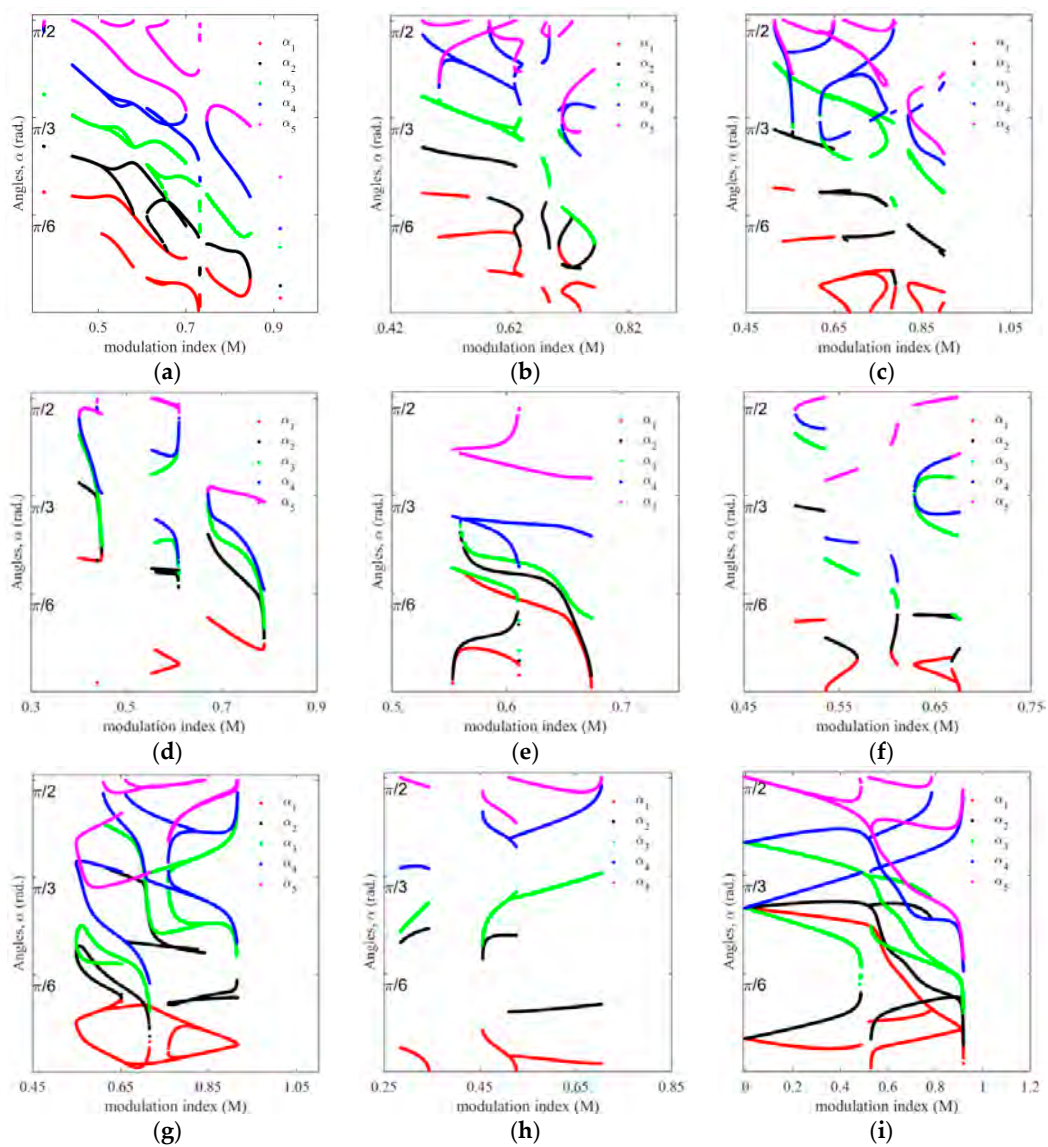


Figure 5. Switching angles (in radians) as function of modulation M for various switching transition (a) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$; (b) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\uparrow}, \alpha_{5\downarrow}$; (c) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\downarrow}, \alpha_{5\uparrow}$; (d) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\downarrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$; (e) $\alpha_{1\uparrow}, \alpha_{2\downarrow}, \alpha_{3\uparrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$; (f) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\uparrow}, \alpha_{4\downarrow}, \alpha_{5\downarrow}$; (g) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\downarrow}, \alpha_{4\uparrow}, \alpha_{5\uparrow}$; (h) $\alpha_{1\uparrow}, \alpha_{2\uparrow}, \alpha_{3\downarrow}, \alpha_{4\downarrow}, \alpha_{5\uparrow}$; (i) $\alpha_{1\uparrow}, \alpha_{2\downarrow}, \alpha_{3\uparrow}, \alpha_{4\downarrow}, \alpha_{5\uparrow}$.

The total harmonics distortion, as a function of the modulation index for the entire pattern, is shown in Figure 6. It clearly shows that there is a wide variation in %THD for different solution sets and patterns. The result for switching angles shows multiple solutions, unique solutions, and no solution in different modulation ranges. When all the patterns are grouped together, a lot of solutions are available to operate the converter, even at a very low modulation index. Selecting a particular option from a number of solutions is normally application-dependent. One can select a particular solution simply based on the lower THD obtained or by taking into account the next low-order non-eliminated harmonics. Other criteria could be based on the minimum switching transition in order to further reduce the power losses in the switches. Based on optimal THD criteria, the optimum switching angles in different ranges of M for all possible patterns of Figure 3 have been given in Figure 6. The switching angles for the range of modulation index of the entire pattern are given and compared in Figure 7. It is evident that there are several options available to operate the inverter in different modulation ranges to obtain the desired performance. From the computational results, it is clear that at a higher modulation value the THD is better than at lower modulation. At a lower modulation range, one can utilize a high switching frequency technique like space vector PWM by operating power switches with hybrid PWM, which could be an active research area. The maximum error in the harmonics function evaluation and the harmonics profile for pattern 'a' are shown in Figure 8. It is evident from the figure that an accurate solution to the SHE equation is obtained and the targeted harmonics are completely eliminated from the output waveform. This is one of the major advantages of utilizing the modified Newton Raphson technique to solve SHE equations.

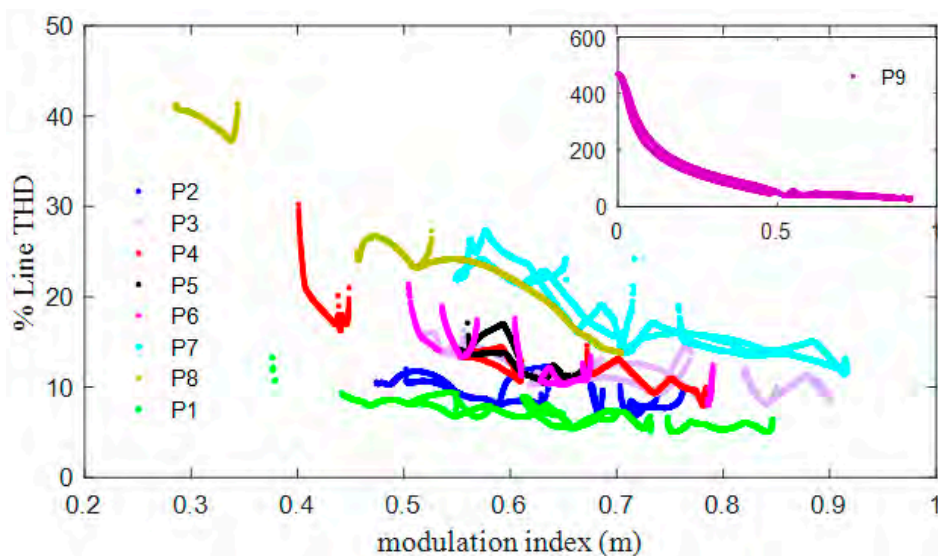


Figure 6. % Line THD for the entire pattern as a function of modulation index M .

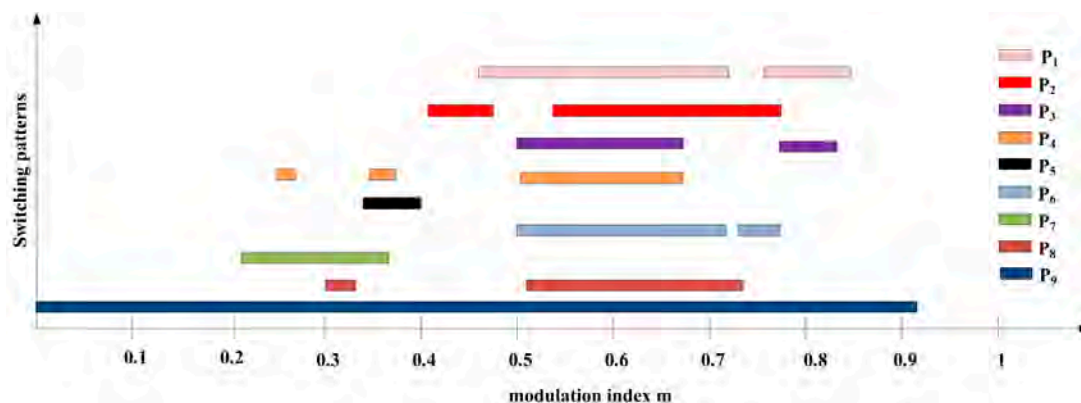


Figure 7. Switching angle as a function of m for all the patterns.

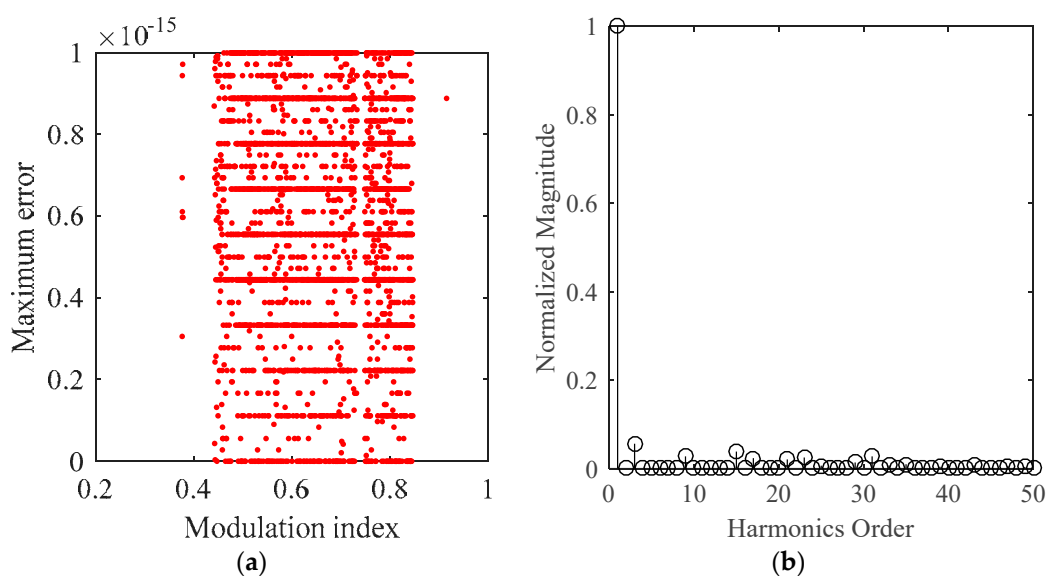


Figure 8. (a) Maximum error in the function for pattern “a”; (b) harmonics profile at $M = 0.845$.

To validate the computational results for switching angles, a simulation is carried out in MATLAB/SIMULINK software tool R2017a (9.2.0.538062) for an 11-level, three-phase cascaded H-bridge inverter. The DC source for each H-bridge unit is considered 100 V. The simulation results cover the whole range of M for the entire pattern. Selected simulation results are represented in Figure 9. The simulation results for phase voltage at modulation index, $M = 0.6$, are shown in Figure 9a, where all the H-bridge cells are producing +100 V at the output. In this case, in a quarter of a full output cycle, the S_{X1} and S_{X3} switches of the first, second, third, fourth, and fifth cells of the first leg are turned on at instant $\alpha_1 = 26.65^\circ$, $\alpha_2 = 43.95^\circ$, $\alpha_3 = 51.56^\circ$, $\alpha_4 = 62.43^\circ$ and $\alpha_5 = 72.54^\circ$, respectively, or at time instants of 1.48 ms, 2.44 ms, 2.86 ms, 3.46 ms, and 4.03 ms, respectively. Similarly, the switches S_{X2} and S_{X3} of the first, second, third, fourth, and fifth cells are turned ON at instant $\alpha_1 = 206^\circ$, $\alpha_2 = 223.95^\circ$, $\alpha_3 = 231.56^\circ$, $\alpha_4 = 242.43^\circ$, and $\alpha_5 = 252.54^\circ$, respectively, or at time instants 11.48 ms, 12.44 ms, 12.86 ms, 13.46 ms, and 14.03 ms. The switches remain turned ON for a duration of 35.19%, 25.58%, 21.35%, 15.32%, and 9.70% of a full cycle, respectively. The simulation results obtained following a similar procedure are in close agreement with the analytical results. Hence it confirms the robustness and correctness of the technique adopted. It can be seen that the low order non-triple harmonics such as 5th, 7th, 11th, and 13th are eliminated from the line-to-line output voltage and the THD is very close to the calculated value.

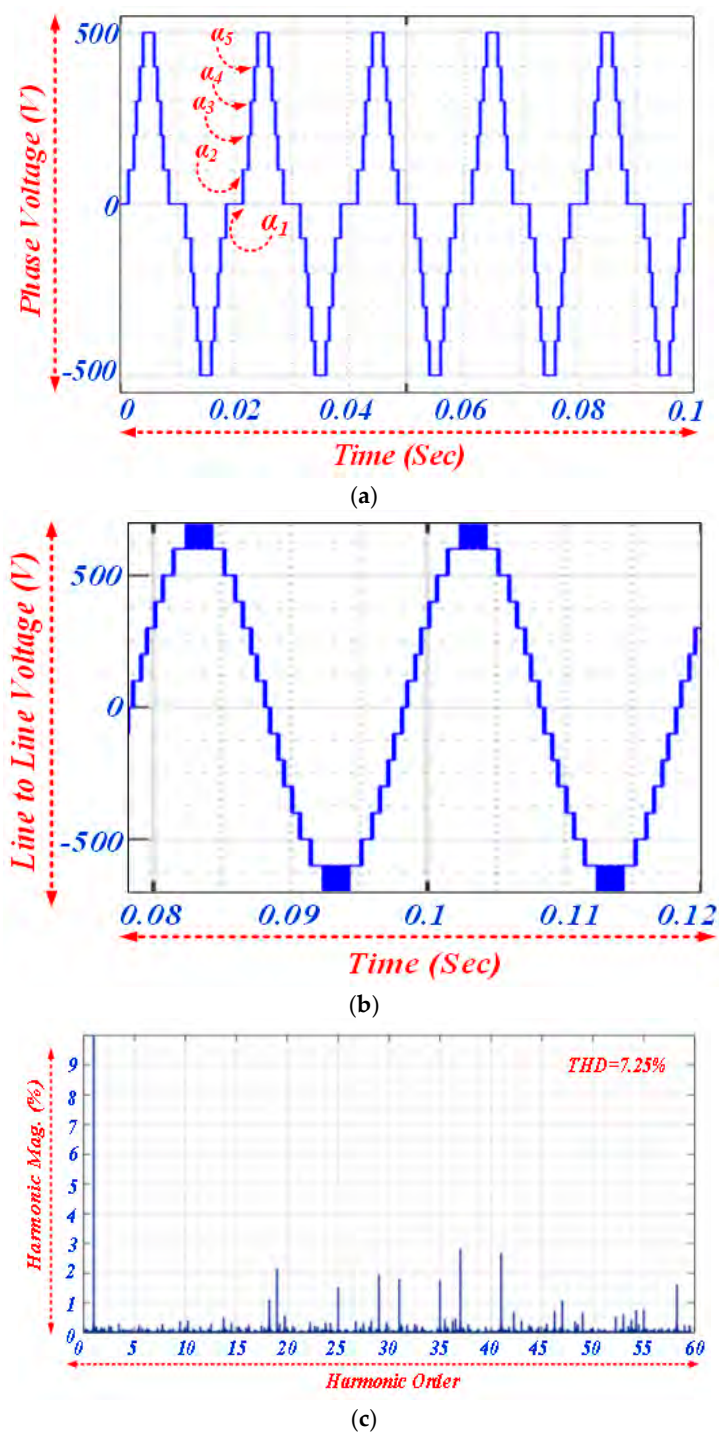


Figure 9. Simulation result for pattern 'a' at $M = 0.6000$ (a) Phase voltage; (b) line voltage; (c) harmonics spectrum.

5. Hardware Setup and Experimental Results

The computational result is validated by a prototype developed in the laboratory. The switches of H-bridge inverter are bidirectional insulated gate bipolar transistors (IGBT) selected from Semikron SKM100GB12T4. The control code for harmonics elimination is built using Xilinx's field-programmable gate array FPGA from VIRTEX-5 XC5VLX50T (Xilinx, San Jose, CA, USA). A harmonics spectrum analyser is also used in conjunction with the scope for FFT analysis. The complete hardware setup is

shown in Figure 10. The switching pulses from FPGA were given to high-speed IGBT gate drivers, which in turn supply a conditioned and proper signal to the IGBT switches.

The DC voltage for each cascaded H-bridge has been kept at 35 V. The first experiment has been carried out for pattern 'a' at modulation index $M = 0.432$ for corresponding switching angles of $\alpha_1 = 0.622$, $\alpha_2 = 0.833$, $\alpha_3 = 1.049$, $\alpha_4 = 1.313$, and $\alpha_5 = 1.561$. Figure 11 shows the output waveform and harmonics spectrum. The time axis is divided into 10 ms/div, while the vertical axis is 49 V/div. The fft spectrum shown confirms that the targeted harmonics for elimination are completely eliminated from the output waveform.

Similarly, the hardware results for 'b' and 'g' are shown in Figures 12 and 13, respectively. The FFT spectrum of these waveforms also shows that the targeted non-triple harmonics (5th, 7th, 11th, and 13th order) considered for elimination are completely absent. In a similar fashion, experimental results can be obtained for the entire modulation range of different possible structures.

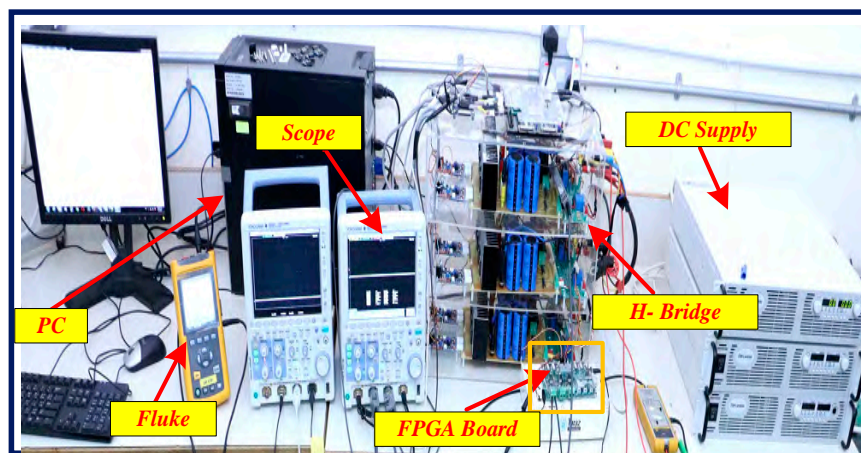


Figure 10. Experimental setup.

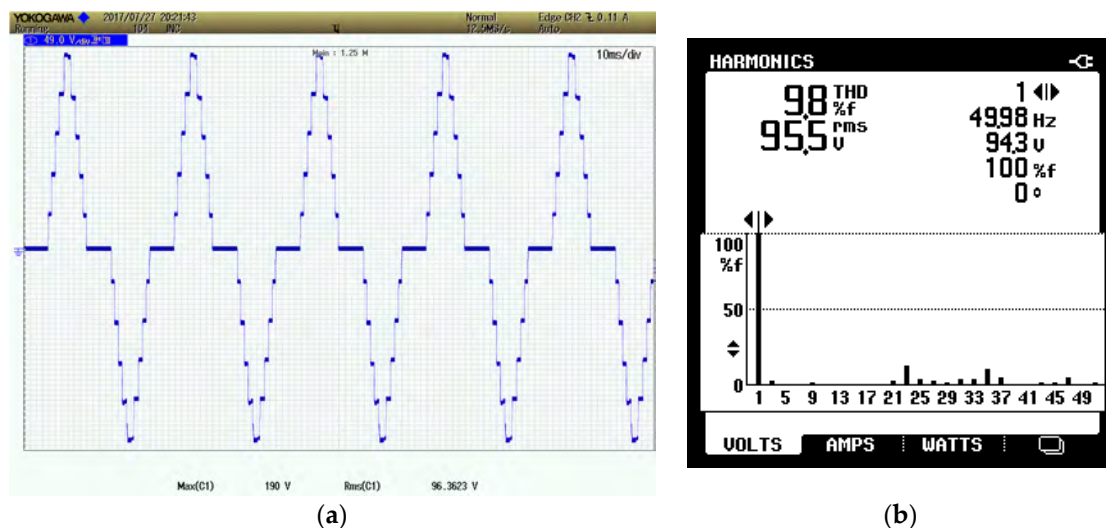


Figure 11. Experimental results for pattern 'a' (a) output voltage waveform at $M = 0.432$; (b) FFT spectrum.

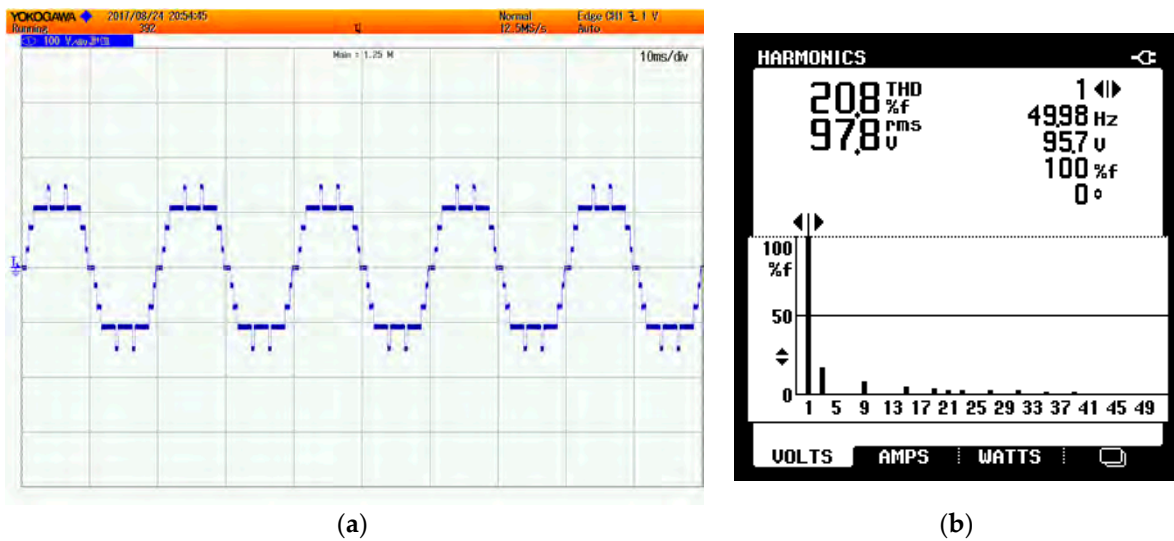


Figure 12. Experimental results of output voltage and THD of pattern of Figure 3b in (a,b) respectively.

A LUT flip flop pair for this architecture represents one LUT paired with one flip flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element. The Figure 14 shows the design summary report for case “a”, which contains device utilization information.

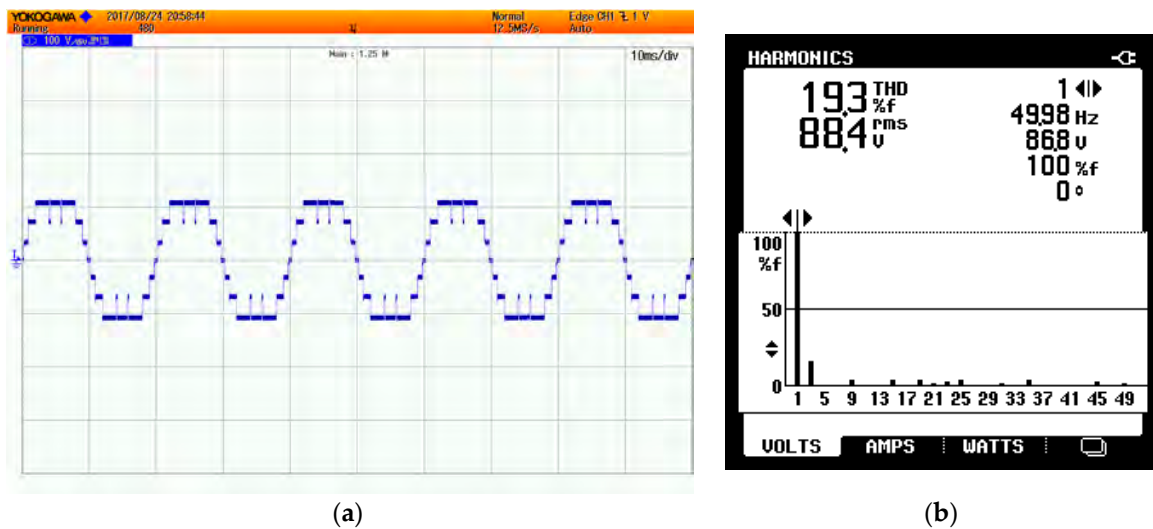


Figure 13. Experimental results of output voltage and THD of pattern of Figure 3c in (a,b) respectively.

uh5_1_cw Project Status (11/22/2015 - 13:46:34)			
Project File:	uh5_1_cw.xise	Parser Errors:	No Errors
Module Name:	uh5_1_cw	Implementation State:	Programming File Generated
Target Device:	xc5vtx50t-1ff1136	•Errors:	No Errors
Product Version:	ISE 14.6	•Warnings:	521 Warnings (327 new)
Design Goal:	Balanced	•Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	All Constraints Met
Environment:	System Settings	•Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	572	28,800	1%	
Number used as Flip Flops	572			
Number of Slice LUTs	704	28,800	2%	
Number used as logic	675	28,800	2%	
Number using O6 output only	554			
Number using O5 output only	61			
Number using O5 and O6	60			
Number used as Memory	22	7,680	1%	
Number used as Shift Register	22			
Number using O6 output only	22			
Number used as exclusive route-thru	7			
Number of route-thrus	89			
Number using O6 output only	68			
Number using O5 output only	21			
Number of occupied Slices	273	7,200	3%	
Number of LUT Flip Flop pairs used	780			
Number with an unused Flip Flop	208	780	26%	
Number with an unused LUT	76	780	9%	
Number of fully used LUT-FF pairs	496	780	63%	
Number of unique control sets	46			
Number of slice register sites lost to control set restrictions	34	28,800	1%	
Number with an unused LUT	76	780	9%	
Number of fully used LUT-FF pairs	496	780	63%	
Number of unique control sets	46			
Number of slice register sites lost to control set restrictions	34	28,800	1%	
Number of bonded IOBs	29	480	6%	
Number of LOCed IOBs	29	29	100%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Average Fanout of Non-Clock Nets	3.44			

Figure 14. Summary report presenting FPGA devices’ utilization.

6. Conclusions

In this paper, two different approaches have been proposed for obtaining multiple sets of solutions in a wide range of modulation indices. The modified NR approach ensures all possible solutions at a particular modulation index, whereas the pattern synthesizing approach ensures coverage of almost the whole range for modulation indices. Selected lower-order non-triple odd harmonics are considered for elimination from the output voltage. The multiple sets of solutions have been found in different ranges of the modulation index, which set are optimal is application-dependent. For instance, one can choose a solution based on optimum THD or one can select a solution based on minimum transition of power switches. From the results it is confirmed that at higher modulation indices the THD is low; however, at very low modulation indices the THD is very high, so further research can be done for hybrid PWM.

However, in some modulation ranges (or in overmodulation), no solution was found. Selected simulation results are presented in this paper to confirm the validity of the theoretical and computational results.

Acknowledgments: This (publication, report, etc.) was made possible by NPRP grant # [X-033-2-007] from the Qatar National Research Fund (a member of Qatar Foundation).

Author Contributions: All authors contributed equally to the proposed research work in its final version to be decimation as full article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wu, A.B. *High-Power Converters and AC Drives*; Wiley-IEEE Press: Hoboken, NJ, USA, 2006.
2. Bharatiraja, C.; Babu, S.; Krishnakumar, V.; Munda, J.L.; Sanjeevikumar, P. Investigation of Slim type BLDC motor Drive with torque ripple minimization using Abridged Space-Vector PWM Control Method. *Int. J. Power Electron. Drive Syst.* **2017**, *8*, 593–600. [[CrossRef](#)]
3. Bharatiraja, C.; Harish, S.; Munda, J.L.; Sanjeevikumar, P.; Kumar, M.S.; Bhati, V. A PWM Strategies for Diode Assisted NPC-MLI to Obtain Maximum Voltage Gain for EV Application. *Int. J. Power Electron. Drive Syst.* **2017**, *8*, 767–774. [[CrossRef](#)]
4. Sanjeevikumar, P.; Grandi, G.; Ojo, J.O.; Blaabjerg, F. Direct Vector Controlled Six-Phase Asymmetrical Induction Motor with Power Balanced Space Vector PWM Multilevel Operation. *Int. J. Power Energy Convers.* **2016**, *7*, 57–83. [[CrossRef](#)]
5. Subramaniam, U.; Arun Shankar, V.K.; Sanjeevikumar, P.; Kandanuru, H. Common Mode Voltage Regulation of Three Phase Three Level Neutral Point Clamped Inverter using SVPWM Technique. In *Advances in Power Systems and Energy Management; Lecture Notes in Electrical Engineering*; Springer Journal Publications: Singapore, 2018; Volume 436, pp. 367–376.
6. Sanjeevikumar, P.; Blaabjerg, F.; Wheeler, P.; Fedák, V.; Duran, M.J.; Siano, P. A Novel Five-level Optimized Carrier Multilevel PWM Quad-Inverter Six-Phase Asymmetrical AC Drive. In Proceedings of the 2016 IEEE International Power Electronics and Motion Control Conference (PEMC), Varna, Bulgaria, 25–28 September 2016.
7. Padmanaban, S.; Siano, P.; Ertas, A.H.; Selvamuthukumar, R.; Maroti, P.K. Single-Phase Seven-Level Stack Multicell Converter Using Level Shifting SPWM Technique. In Proceedings of the 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC), Florence, Italy, 7–10 June 2016.
8. Pandav, K.M.; Mahajan, S.B.; Sanjeevikumar, P.; Badave, S.M.; Pachagade, R.M. 2.4 kW Three Phase Inverter for Aircraft Application- Hardware Implementation. In *Advances in Power Systems and Energy Management; Lecture Notes in Electrical Engineering Book*; Springer: Singapore, 2016.
9. Padmanaban, S.; Blaabjerg, F.; Wheeler, P.W.; Ojo, J.O.; Maroti, P.K. A Novel Double Quad-Inverter Configuration for Multilevel Twelve-Phase Open-Winding Converter. In Proceedings of the 2016 IEEE 6th International Conference on Power Systems (ICPS), Delhi, India, 4–6 March 2016.
10. Padmanaban, S.K.; Bhaskar, M.S.; Maroti, P.K.; Blaabjerg, F.; Siano, P.; Oleschuk, V. Hexuple-Inverter Configuration for Multilevel Nine-Phase Symmetrical Open-Winding Converter. In Proceedings of the IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, India, 4–6 July 2016.
11. Abu-Rub, H.; Iqbal, A.; Guzinski, J. *High Performance Control of AC Drives with Matlab/Simulink Models*; John Wiley and Sons: Hoboken, NJ, USA, 2012.
12. Hosseyni, A.; Trabelsi, R.; Iqbal, A.; Padmanaban, S.; Mimouni, M.F. An Improved Sensorless Sliding Mode Control/Adaptive Observer of a Five-Phase Permanent Magnet Synchronous Motor Drive. *Int. J. Adv. Manuf. Technol.* **2017**, *93*, 1029–1039. [[CrossRef](#)]
13. Dahidah, M.S.; Konstantinou, G.; Agelidis, V.G. A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications. *IEEE Trans. Power Electron.* **2015**, *30*, 4091–4106. [[CrossRef](#)]
14. Wei, Q.; Wu, B.; Xu, D.; Zargari, N.R. A Natural-Sampling-Based SVM Scheme for Current Source Converter with Superior Low-Order Harmonics Performance. *IEEE Trans. Power Electron.* **2016**, *31*, 6144–6154. [[CrossRef](#)]
15. Feng, Z.; Guangzhen, Z.; Xuhui, W.; Li, Z. A novel implementation of harmonic elimination pulse width modulation technique. In Proceedings of the 2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), Beijing, China, 31 August–3 September 2014.

16. Chiasson, J.N.; Tolbert, L.M.; McKenzie, K.J.; Du, Z. A new approach to solving the harmonic elimination equations for a multilevel converter. In Proceedings of the 38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, Salt Lake City, UT, USA, 12–16 October 2003; pp. 640–647.
17. Yang, K.; Chen, L.; Zhang, J.; Hao, J.; Yu, W. Parallel resultant elimination algorithm to solve the selective harmonic elimination problem. *IET Power Electron.* **2016**, *9*, 71–80. [[CrossRef](#)]
18. Yang, K.; Zhang, Q.; Yuan, R.; Yu, W.; Yuan, J.; Wang, J. Selective Harmonic Elimination with Groebner Bases and Symmetric Polynomials. *IEEE Trans. Power Electron.* **2016**, *31*, 2742–2752. [[CrossRef](#)]
19. Ozpineci, B.; Tolbert, L.M.; Chiasson, J.N. Harmonic Optimization of Multilevel Converters Using Genetic Algorithms. *IEEE Power Electron. Lett.* **2005**, *3*, 92–95. [[CrossRef](#)]
20. TarafdarHagh, M.; Taghizadeh, H.; Razi, K. Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization. *IEEE Trans. Power Electron.* **2009**, *24*, 2259–2267.
21. Taghizadeh, H.; Hagh, M.T. Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization. *IEEE Trans. Ind. Electron.* **2010**, *57*, 3678–3684. [[CrossRef](#)]
22. Sundareswaran, S.; Jayant, K.; Shanavas, T.N. Inverter Harmonic Elimination through a Colony of Continuously Exploring Ants. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2558–2565. [[CrossRef](#)]
23. Filho, F.; Tolbert, L.M.; Cao, Y.; Ozpineci, B. Real-time selective harmonic minimization for multilevel inverters connected to solar panels using artificial neural network angle generation. *IEEE Trans. Ind. Appl.* **2011**, *47*, 2117–2124. [[CrossRef](#)]
24. Etesami, M.H.; Farokhnia, N.; Fathi, S.H. Toward Harmonic Minimization in Multilevel Inverters. *IEEE Trans. Ind. Inform.* **2015**, *11*, 459–466.
25. Kavousi, A.; Vahidi, B.; Salehi, R.; Bakhshizadeh, M.K.; Farokhnia, N.; Fathi, S.H. Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters. *IEEE Trans. Power Electron.* **2012**, *27*, 1689–1696. [[CrossRef](#)]
26. Wang, J.; Ahmadi, D. A precise and practical harmonic elimination method for multilevel inverters. *IEEE Trans. Ind. Appl.* **2010**, *46*, 857–865. [[CrossRef](#)]
27. Dahidah, M.S.; Agelidis, V.G. Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters: A Generalized Formula. *IEEE Trans. Power Electron.* **2008**, *23*, 1620–1630. [[CrossRef](#)]
28. Napoles, J.; Leon, J.I.; Franquelo, L.G.; Portillo, R.; Aguirre, M.A. Selective harmonic mitigation technique for multilevel cascaded H-bridge converters. In Proceedings of the 2009 35th Annual Conference of IEEE Industrial Electronics, Porto, Portugal, 3–5 November 2009; pp. 806–811.
29. Zhao, H.; Jin, T.; Wang, S.; Sun, L. A Real-Time Selective Harmonic Elimination Based on a Transient-Free Inner Closed-Loop Control for Cascaded Multilevel Inverters. *IEEE Trans. Power Electron.* **2016**, *31*, 1000–1014. [[CrossRef](#)]
30. Aleenejad, M.; Mahmoudi, H.; Moamaei, P.; Ahmadi, R. A new fault-tolerant strategy based on a modified selective harmonic technique for three-phase multilevel converters with a single faulty cell. *IEEE Trans. Power Electron.* **2016**, *31*, 3141–3150. [[CrossRef](#)]
31. Banaei, M.R.; Shayan, P.A. Solution for selective harmonic optimisation in diode-clamped inverters using radial basis function neural networks. *IET Power Electron.* **2014**, *7*, 1797–1804. [[CrossRef](#)]
32. Massrur, H.R.; Niknam, T.; Mardaneh, M. Harmonic Elimination in Multilevel Inverters under Unbalanced Voltages and Switching Deviation Using a New Stochastic Strategy. *IEEE Trans. Ind. Inform.* **2016**, *12*, 716–725. [[CrossRef](#)]
33. Grandi, G.; Sanjeevikumar, P.; Ostojic, D.; Rossi, C. Quad-inverter configuration for multi-phase multi-level ac motor drives. In Proceedings of the 2010 IEEE Region 8 International Conference on Computational Technologies in Electrical and Electronics Engineering (SIBIRCON), Irkutsk Listvyanka, Russia, 11–15 July 2010; pp. 631–638.
34. Grandi, G.; Tani, A.; Sanjeevikumar, P.; Ostojic, D. Multi-phase multi-level ac motor drive based on four three-phase two-level inverters. In Proceedings of the 2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM), Pisa, Italy, 14–16 June 2010; pp. 1768–1775.
35. Rasool, A.; Ozsoy, E.E.; Ahmad, F.; Sabanovic, A.; Padmanaban, S. Disturbance-Observer Based Control of Voltage-Source-Converter under Unbalanced Voltage Conditions. *World J. Eng.* **2017**, *14*, 522–553. [[CrossRef](#)]

