IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Pulse width modulation technique for a three-to-five phase matrix converter with reduced commutations

ISSN 1755-4535
Received on 7th January 2015
Revised on 10th July 2015
Accepted on 22nd July 2015
doi: 10.1049/iet-pel.2015.0015
www.ietdl.org

Mahmoud A. Sayed[1] ✉, *Atif Iqbal*[2]

[1]*Electrical Engineering Department, Faculty of Engineering, South Valley University, Qena, Egypt*
[2]*Department of Electrical Engineering, Qatar University, Doha, Qatar*
✉ *E-mail: mahmoud_sayed@ieee.org*

Abstract: Variable-speed multiphase drive systems have become an increasingly important topics compared with conventional three-phase one due to their distinct advantages. This study presents a new pulse width modulation (PWM) technique for controlling the three-to-five phase matrix converter to reduce the commutation number of the power switches and the total harmonic distortion, simultaneously. The proposed PWM technique provides full output voltage and frequency control in addition to unity input power factor by changing only five switch states during the control period. Moreover, it prevents direct switching or commutation between the maximum and minimum input voltages to reduce the switches voltage stress. Moreover, the proposed PWM technique provides output voltage ratio equal to 78.86% of the input voltage. The effectiveness of the proposed control scheme has been verified theoretically by using PSIM software and experimentally by using a laboratory prototype.

1 Introduction

Recently, the need for power converters in the industrial applications has attracted much attention worldwide. The AC/AC power converters are commonly classified into indirect and direct systems [1, 2]. The most commonly indirect AC/DC/AC converters are used for variable voltage and frequency supply, as shown in Fig. 1*a*. The first converter stage converts the input AC power to DC, and then the DC power is reconverted to AC with controlled amplitude and frequency by using the second stage. On the other hand, direct AC/AC converters provide direct AC to AC power conversion, as shown in Fig. 1*b*. Direct AC/AC converters have attracted much attention since no intermediate energy conversion stage is used. This is also called the matrix converter that offer several advantages when compared with back-to-back converter (converter with active front end converter and an inverter). Matrix converter enables the bi-directional power flow between the power supply and the load. Since it has only one power stage, there is no need for the bulky and short life-time electrolytic capacitor. It also has the ability to control the output voltage magnitude and frequency in addition to operating at unity input power factor for any load. The disadvantages of this converter topology is the control complexity due to large number of switching devices and bi-directional power flow control. A comprehensive overview of the developments in matrix converter is presented in [3–6].

Multiphase (more than three phases) machines have growing interests in the applications that consider reliability as a prime target. Therefore, the need for multiphase converters to supply such multiphase systems is becoming a new challenge. The research on multiphase drive systems has been significantly developed due to advancement in semi-conductor devices and digital signal processors technologies. Multiphase drives possess several advantages over conventional three-phase drives such as: reducing the amplitude and increasing the frequency of torque pulsations, reducing the rotor harmonic currents, reducing the current per phase without increasing the voltage per phase, lowering the harmonics and higher reliability. A comprehensive literature review on the state-of-art in multiphase drives is presented in [7–13]. In general, multiphase machines are driven by using multiphase AC/DC/AC converters with carrier-based pulse width modulation (PWM) or space vector PWM control [14–17]. However, matrix converter has recently been considered in the applications of multiphase systems. Different phase numbers of outputs are reported in the literature such as three-phase input five-phase output [18, 19], three-phase input six-phase output [20], three-phase input seven-phase output [21, 22] and three-phase input nine-phase output [23].

Due to the large number of bi-directional switches in the matrix converter, numerous PWM techniques are proposed and reported in the literature. In the 3×3 matrix converter, at the beginning, Alesina and Venturini [24] presented scalar PWM technique with output equal to 50% of the input. The PWM was improved by proposing harmonic injection based scheme that increased the output to 86.6% of the input [25]. The same output voltage ratio was presented by Roy's method [26]. Space vector PWM was further presented for 3×3 matrix converter with output equal to 86.6% [27]. For three-phase input and multiphase output matrix converter, several PWM schemes are available in literature such as carrier-based with harmonic injection [28], direct duty ratio based PWM [29] and space vector PWM [18]. Space vector PWM is considered as one of the most popular PWM because of their easier digital realisation and giving insight into the PWM process. When applied to matrix converter with multiphase output, it offers lot of flexibility in choosing space vectors from large set of available vectors and many of them are redundant. On one hand this flexibility will offer better control characteristics, while on the other hand this is highly complex optimisation problem. Table 1 summarises the PWM switching techniques of the 3×3 and 3×5 matrix converters along with the required bi-directional switches and the voltage transfer ratio v_o/v_i of each method.

In this paper, a new PWM technique is proposed for controlling the three-to-five phase matrix converter. The proposed method provides low total harmonic distortion (THD) in the output line-to-line voltage and reduces the commutation number during the switching period. Although the matrix converter has 15 switches, the commutation number is only five in one switching period in contrast to space vector PWM that needs ten commutations. Besides, it provides low voltage switching stress by changing the switches state at minimum voltage drop. It also provides full control of the input power factor in addition to output voltage magnitude and frequency. The effectiveness of the proposed PWM switching technique has been verified experimentally.

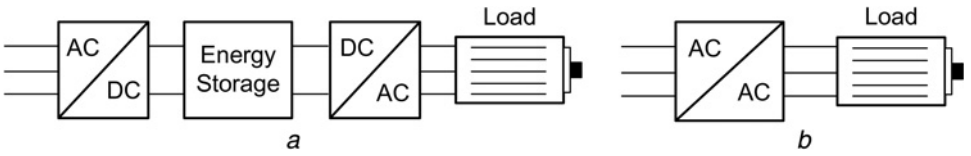

Fig. 1 *AC/AC converters*

a Indirect converters
b Direct converters

2 Three-to-five phase matrix converter model

Fig. 2 shows the basic circuit configuration of the three-to-five phase matrix converter. This matrix converter has 15 bi-directional switches connecting the three-phase input side with the five-phase output side. This configuration allows any output phase to be connected with any input phase. The three-phase input terminals are usually connected to a three-phase voltage supply, whereas the five-phase terminals are usually connected to a five-phase inductive load. The input side has 120° phase displacement, whereas the output side has 72° phase displacement between each phase. It is necessary to install LC filter at the input side to smooth the current waveform. However, it can be neglected in this section to focus only on the mathematical model.

The three-phase input voltages e_r, e_s and e_t are given using the rms line voltage E and the displacement angle θ as follows:

$$\begin{bmatrix} e_r \\ e_s \\ e_t \end{bmatrix} = \sqrt{\frac{2}{3}}E \begin{bmatrix} \cos\theta \\ \cos(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) \end{bmatrix} \tag{1}$$

The line-to-line input voltage can be formulated as follows:

$$\begin{bmatrix} e_{rs} \\ e_{st} \\ e_{tr} \end{bmatrix} = \begin{bmatrix} e_r - e_s \\ e_s - e_t \\ e_t - e_r \end{bmatrix} = \sqrt{2}E \begin{bmatrix} \cos(\theta + \pi/6) \\ \cos(\theta - \pi/2) \\ \cos(\theta - 7\pi/6) \end{bmatrix} \tag{2}$$

$$\theta = \omega t + \varphi_0 \tag{3}$$

where ω and φ_0 are the angular frequency and an arbitrary angle of the source voltage, respectively. Unit input current references, which are in-phase with the input phase voltages, are used to achieve unity input power factor. Therefore, the unit input current references i_{ir}^*, i_{is}^* and i_{it}^* are defined using the input reference phase angle φ^* as follows;

$$\begin{bmatrix} i_{ir}^* \\ i_{is}^* \\ i_{it}^* \end{bmatrix} = \begin{bmatrix} \cos(\theta + \varphi^*) \\ \cos(\theta + \varphi^* - 2\pi/3) \\ \cos(\theta + \varphi^* + 2\pi/3) \end{bmatrix} \tag{4}$$

The reference unit input current, given in (4), is used only to control the unity input power factor. According to (1) and (4), the unit input power P_i can be formulated as follows:

$$P_i = e_r i_{ir}^* + e_s i_{is}^* + e_t i_{it}^* \tag{5}$$

The output reference phase voltages v_a^*, v_b^*, v_c^*, v_d^* and v_e^* are defined using line voltage rms V_L^* and argument θ_L^* by:

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \\ v_d^* \\ v_e^* \end{bmatrix} = \frac{\sqrt{2}}{k} V_L^* \begin{bmatrix} \cos\theta_L^* \\ \cos(\theta_L^* - 2\pi/5) \\ \cos(\theta_L^* - 4\pi/5) \\ \cos(\theta_L^* - 6\pi/5) \\ \cos(\theta_L^* - 8\pi/5) \end{bmatrix} \tag{6}$$

$$k = \frac{\sin(2\pi/5)}{\sin(3\pi/10)}, \quad \theta_L^* = \omega_L^* t + \varphi_L^* \tag{7}$$

where k is a factor obtained from the relation between the line and phase voltages of the five-phase system, ω_L^* and φ_L^* are the angular frequency and an arbitrary angle of the output voltage reference. From (6), the output line voltage references v_{ab}^*, v_{bc}^*, v_{cd}^*, v_{de}^* and v_{ea}^* are defined by:

$$\begin{bmatrix} v_{ab}^* \\ v_{bc}^* \\ v_{cd}^* \\ v_{de}^* \\ v_{ea}^* \end{bmatrix} = \begin{bmatrix} v_a^* - v_b^* \\ v_b^* - v_c^* \\ v_c^* - v_d^* \\ v_d^* - v_e^* \\ v_e^* - v_a^* \end{bmatrix} = \sqrt{2}V_L^* s \begin{bmatrix} \cos(\theta_L^* + 3\pi/10) \\ \cos(\theta_L^* - \pi/10) \\ \cos(\theta_L^* - 5\pi/10) \\ \cos(\theta_L^* - 9\pi/10) \\ \cos(\theta_L^* - 13\pi/10) \end{bmatrix} \tag{8}$$

The duty cycles $D_{ra} - D_{te}$ of the 15 bi-directional switches $S_{ra} - S_{te}$ should be decided to realise the reference output voltages and unity

Table 1 Summary of 3 × 3 and 3 × 5 matrix converters

Type of MC	No. of IGBTs	PWM methods	Max. v_o/v_i
3 × 3	9	Venturini	0.5
		modified Venturini	0.867
		Roy	0.867
		carrier modulation	0.5
		carrier modulation (harmonic injection)	0.867
		space vector	0.867
3 × 5	15	carrier modulation	0.5
		carrier modulation (3rd harmonic injection)	0.75
		carrier modulation (3rd and 5th harmonic injection)	0.7886
		space vector	0.7886

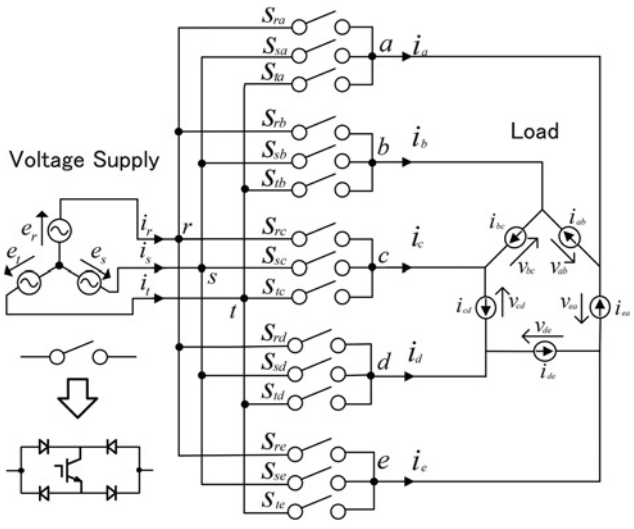

Fig. 2 *Three-to-five phase matrix converter*

input power factor. All switches duty cycles can be formulated based on the following constraints:

$$D_{lm} = \frac{T_{lm}}{T} \quad l = \{r, s, t\} \quad m = \{a, b, c, d, e\} \tag{9}$$

$$D_{rm} + D_{sm} + D_{tm} = 1 \quad m = \{a, b, c, d, e\} \tag{10}$$

3 Proposed switching pattern

The proposed switching pattern has been developed to meet the following objectives:

- Reducing the commutation number and THD.
- Controlling the load voltage magnitude and frequency.
- Achieving unity input power factor regardless of the load type.

In three-to-five phase matrix converter, the input voltage is three-phase shifted by 120°, whereas the output voltage is five-phase shifted by 72°. Fig. 3 shows the three-phase and five-phase waveforms. It is clear that the three-phase input voltage has three levels, whereas the five-phase output voltage has five levels. The levels of the input phase voltages are defined as maximum, middle, and minimum that changes every 60°. The levels of the output phase voltages are defined as maximum, mid-high, middle, mid-low, and minimum that changes every 36°.

Fig. 4*a* shows the proposed switching pattern of the three-to-five phase matrix converter. The proposed pattern is explained considering the input voltages $e_r > e_s > e_t$ during input phase angle ($0 \le \theta \le \pi/3$) and reference output voltages $v_a^* > v_b^* > v_e^* > v_c^* > v_d^*$ during output phase angle ($0 \le \theta_L \le \pi/5$). Therefore, the levels of the input voltages e_r, e_s and e_t are maximum, middle and minimum, respectively. Moreover, the levels of the output voltages v_a^*, v_b^*, v_e^*, v_c^* and v_d^* are maximum, mid-high, middle, mid-low and minimum, respectively. The proposed technique is designed based on minimum voltage drop switching (MVDS), which prevents the direct switching between maximum and minimum input voltage when realising the reference load voltage. Moreover, the commutation number during the control period T is five, which is half of that 10 commutation needed in case of using space vector modulation (SVM) technique. Therefore, the MVDS reduces the voltage stress on power switches and hence increase the converter efficiency.

According to the proposed switching pattern, Fig. 4*b* shows the estimated five-phase output line voltages during the control period T. The maximum and mid-high reference voltage levels (v_a^* and v_b^*) are realised by switching the output phases (a and b) only with the input phases (r and s) that have maximum and middle voltage levels (v_r and v_s). Moreover, the mid-low reference voltage level (v_c^*) is realised by switching the output phases (c) only with the input phases (s and t) that have middle and minimum voltage levels (v_s and v_t). The output phase (d), which has the minimum

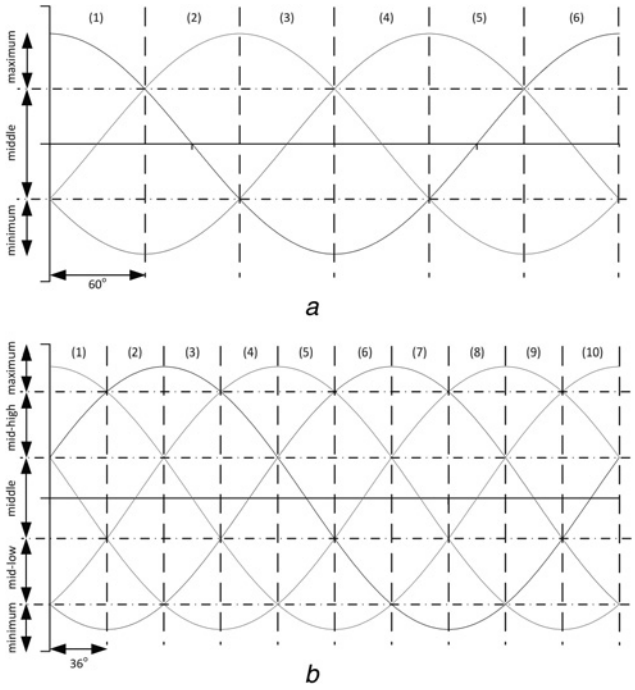

Fig. 3 *Time intervals and voltage levels of the three and five phase waveforms*

a Time intervals and voltage levels of the three-phase waveforms
b Time intervals and voltage levels of the five-phase waveforms

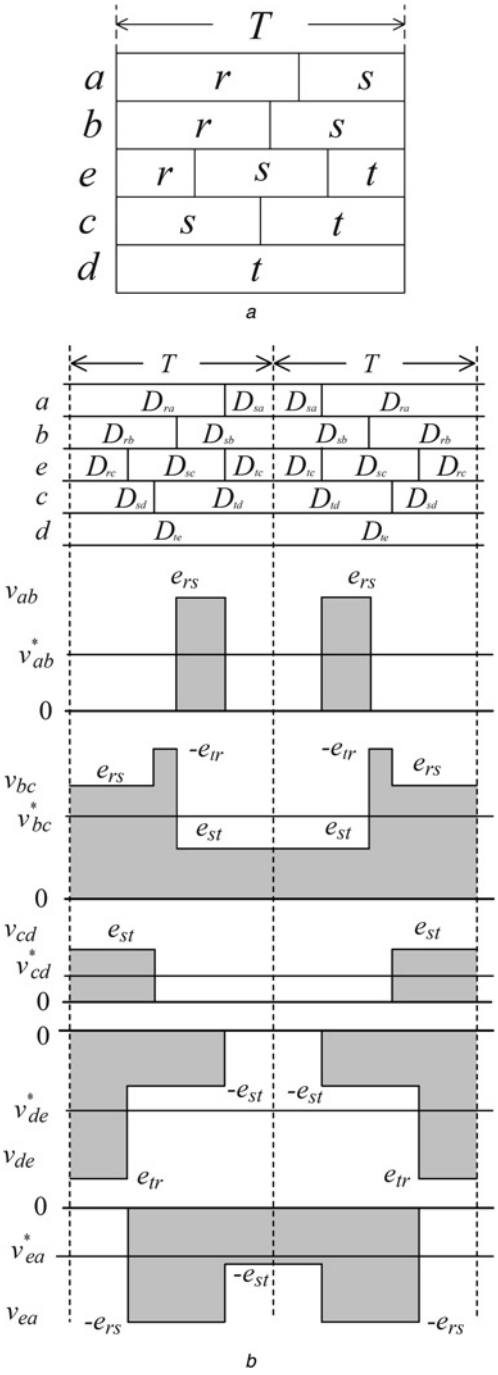

Fig. 4 *Proposed switching pattern of the matrix converter*

a PWM switching pattern
b Estimated output voltage during switching period

IET Power Electron., 2016, Vol. 9, Iss. 3, pp. 466–475

reference voltage level (v_d^*), is always connected to the input phase that has the minimum voltage level (v_t). The middle reference voltage level (v_e^*) is realised by switching the output phase (e) with all input phases of maximum, middle, and minimum voltage levels. Therefore, there is no direct switching between the maximum and minimum voltage levels of the input and output phases.

4 Matrix converter duty cycles

4.1 Duty cycles calculations

Duty cycle calculations are done according to the equivalent circuits of the three-to-five phase matrix converter and the proposed PWM technique. The duty cycle calculations and the equivalent circuits are explained in case of input voltages $e_r > e_s > e_t$ and output voltage references $v_a^* > v_b^* > v_e^* > v_c^* > v_d^*$. Fig. 5 shows the equivalent circuits of the three-to-five phase matrix converter according to the proposed switching pattern. It is clear that the switching frequency of the converter is much higher than the frequency of the input and output voltage and currents. Therefore, during the control period T, input and output voltages and currents are assumed to be constant.

4.1.1 Duty cycles of middle and minimum voltage phases: Duty cycles of all switches connecting phase (e) and phase (d) are calculated based on the equivalent circuit shown in Figs. 5*a* and *b*. Since phase (e) is the middle output voltage level, it is controlled by the switches (S_{re}, S_{se} and S_{te}), allowing phase (e) to be switched with all input voltage levels; phase (r), phase (s) and phase (t). phase (a) is the maximum output voltage level, which is controlled by the two switches (S_{ra} and S_{sa}), allowing phase (a) to be switched with only the maximum and middle input voltage levels, phase (r) and phase (s), respectively. The average three-phase input current can be formulated as a function of the reference unit input current, given in (4), as follows:

$$\begin{bmatrix} \bar{i}_{rea} \\ \bar{i}_{sea} \\ \bar{i}_{tea} \end{bmatrix} = K_{ea} \begin{bmatrix} i_{ir}^* \\ i_{is}^* \\ i_{it}^* \end{bmatrix} \tag{11}$$

The input power during the control period T can be formulated as follows:

$$P_{ea} = K_{ea}(e_r i_{ir}^* + e_s i_{is}^* + e_t i_{it}^*) = K_{ea} * P_{\mathrm{i}} \tag{12}$$

where, the P_{i} is the unit input power. Assuming ideal converter, the output current can be formulated as follows:

$$i_{ea} = \frac{K_{ea} P_{\mathrm{i}}}{v_{ea}^*} \tag{13}$$

The duty cycle of the switch S_{te} can be formulated as follows:

$$D_{te} = \frac{i_{tea}}{i_{ea}} = \frac{i_{it}^* v_{ea}^*}{P_{\mathrm{i}}} \tag{14}$$

Phase (d) in Fig. 5*b*, which is the minimum output voltage level, is connected only to the minimum level input voltage, phase (t), through the switch (S_{td}). The average three-phase input current can be formulated as follows:

$$\begin{bmatrix} \bar{i}_{rde} \\ \bar{i}_{sde} \\ \bar{i}_{tde} \end{bmatrix} = K_{de} \begin{bmatrix} i_{ir}^* \\ i_{is}^* \\ i_{it}^* \end{bmatrix} \tag{15}$$

The input power during the control period T can be formulated as follows:

$$P_{de} = K_{de}(e_r i_{ir}^* + e_s i_{is}^* + e_t i_{it}^*) = K_{ea} * P_{\mathrm{i}} \tag{16}$$

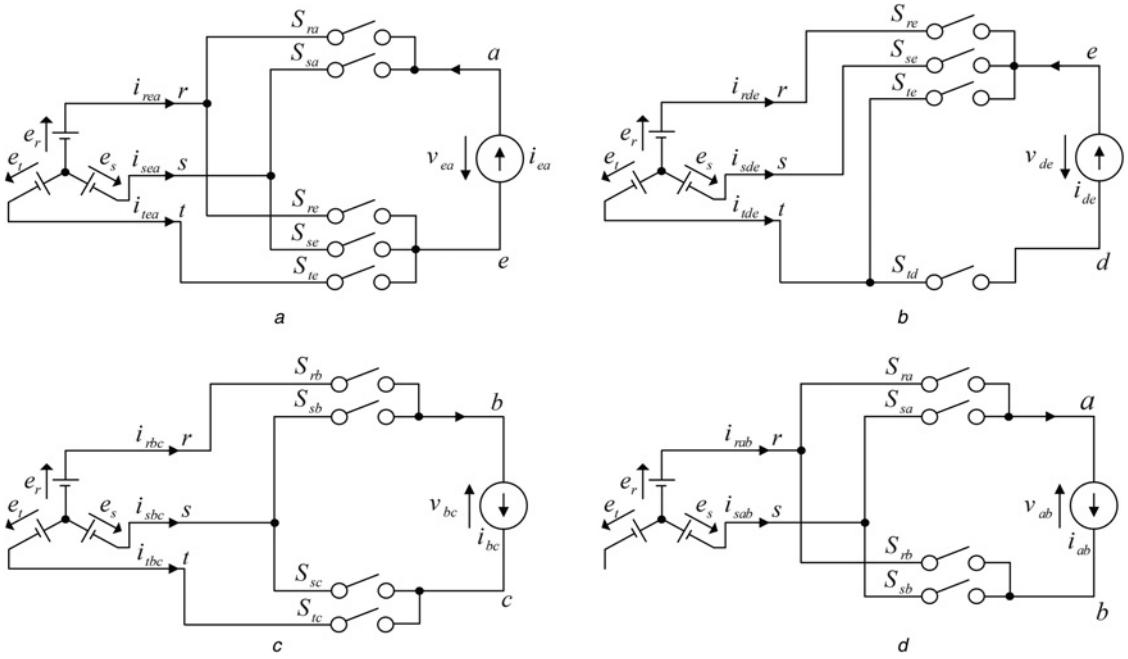

Fig. 5 *Circuit diagram of the proposed switching pattern*

a Connection of the maximum and middle voltage phases
b Connection of the middle and minimum voltage phases
c Connection of the mid-high and mid-low voltage phases
d Connection of the maximum and mid-high voltage phases

Therefore, the output current can be formulated as follows:

$$i_{de} = \frac{K_{de} P_{\mathrm{i}}}{v^*_{de}} \tag{17}$$

The duty cycle of the switch S_{re} can be formulated as follows:

$$D_{re} = \frac{-i_{rde}}{i_{de}} = \frac{-i^*_{ir} v^*_{de}}{P_{\mathrm{i}}} \tag{18}$$

The duty cycle of the switch S_{re}, shown in 18, is always positive since the voltage v^*_{de} is always negative and the maximum unit input current i^*_{ir} is always positive. Based on 14 and 18, the duty cycle of the switch S_{se} can be formulated as follows:

$$D_{se} = 1 - \frac{i^*_{it} v^*_{ea} - i^*_{ir} v^*_{de}}{P_{\mathrm{i}}} \tag{19}$$

Since there is no switching between phase (d) and both of phase (r) and phase (s), the duty cycles of S_{rd} and S_{sd} are zero. Therefore, the duty cycle of the switch S_{td} is one.

4.1.2 Duty cycles of mid-high and mid-low voltage phases: Duty cycles of all switches connecting phase (b) and phase (c) are calculated based on the equivalent circuit shown in Fig. 5*c*. Since phase (b) is the mid-high output voltage level, it is controlled by the two switches (S_{rb} and S_{sb}), allowing phase (b) to be switched with only the maximum and middle input voltage levels, phase (r) and phase (s), respectively. Phase (c), the mid-low output voltage level, is controlled by the two switches (S_{sc} and S_{tc}), allowing phase (c) to be switched with only the middle and minimum input voltage levels, phase (s) and phase (t), respectively. The average three-phase input current can be formulated as follows:

$$\begin{bmatrix} \bar{i}_{rbc} \\ \bar{i}_{sbc} \\ \bar{i}_{tbc} \end{bmatrix} = K_{bc} \begin{bmatrix} i^*_{ir} \\ i^*_{is} \\ i^*_{it} \end{bmatrix} \tag{20}$$

The input power during the control period T is:

$$P_{bc} = K_{bc}(e_r i^*_{ir} + e_s i^*_{is} + e_t i^*_{it}) = K_{bc} * P_{\mathrm{i}} \tag{21}$$

Therefore, the output current can be formulated as follows:

$$i_{bc} = \frac{K_{bc} P_{\mathrm{i}}}{v^*_{bc}} \tag{22}$$

The duty cycle of the switch S_{rb} can be formulated as follows:

$$D_{rb} = \frac{i_{rbc}}{i_{bc}} = \frac{i^*_{ir} v^*_{bc}}{P_{\mathrm{i}}} \tag{23}$$

Since there is no connection between phase (b) and phase (t), the duty cycle of the switch S_{tb} is zero. Therefore, the duty cycle of the switch S_{sb} can be formulated as follows:

$$D_{sb} = 1 - \frac{i^*_{ir} v^*_{bc}}{P_{\mathrm{i}}} \tag{24}$$

By using the same technique, the duty cycle of the switch S_{tc} can be formulated as follows:

$$D_{tc} = -\frac{i_{tbc}}{i_{bc}} = -\frac{i^*_{it} v^*_{bc}}{P_{\mathrm{i}}} \tag{25}$$

Since there is no connection between phase (c) and phase (r), the duty cycle of the switch S_{rc} is zero. Therefore, the duty cycle of the switch S_{sc} can be formulated as follows:

$$D_{sc} = 1 + \frac{i^*_{it} v^*_{bc}}{P_{\mathrm{i}}} \tag{26}$$

4.1.3 Duty cycles of maximum voltage phase: Phase (a), the maximum output voltage level, is controlled by the two switches (S_{ra} and S_{sa}). Therefore, the duty cycles of all switches controlling phase (a) are calculated based on the equivalent circuit shown in Fig. 5*d*. The average input current can be formulated as follows:

$$\begin{bmatrix} \bar{i}_{rab} \\ \bar{i}_{sab} \\ \bar{i}_{tab} \end{bmatrix} = K_{ab} \begin{bmatrix} i^*_{ir} \\ i^*_{is} \\ i^*_{it} \end{bmatrix} \tag{27}$$

Moreover, the load current can be formulated as follows:

$$i_{ab} = \frac{K_{ab} P_{\mathrm{i}}}{v^*_{ab}} \tag{28}$$

Therefore, the duty cycle of the switch S_{sa} can be formulated based on that of switch S_{sb}, given in (24), as follows:

$$D_{sa} = D_{sb} + \frac{i^*_{is} v^*_{ab}}{P_{\mathrm{i}}} = 1 - \frac{i^*_{ir}(v^*_{ab} + v^*_{bc})}{P_{\mathrm{i}}} \tag{29}$$

Since there is no switching between phase (a) and phase (t), the duty cycle of the switch S_{ta} is zero. Therefore, the duty cycle of the switch S_{ra} can be formulated as follows:

$$D_{ra} = \frac{i^*_{ir}(v^*_{ab} + v^*_{bc})}{P_{\mathrm{i}}} \tag{30}$$

Table 2 Input voltages and currents relationship

Phase angle	Phase voltages			Line voltage signs			Source currents		
θ	e_r	e_s	e_t	e_{rs}	e_{st}	e_{tr}	i^*_r	i^*_s	i^*_t
$0 \sim \pi/3$	e_1	e_2	e_3	+	+	−	max	mid	min
$\pi/3 \sim 2\pi/3$	e_2	e_1	e_3	−	+	−	mid	max	min
$2\pi/3 \sim \pi$	e_3	e_1	e_2	−	+	+	min	max	mid
$\pi \sim 4\pi/3$	e_3	e_2	e_1	−	−	+	min	mid	max
$4\pi/3 \sim 5\pi/3$	e_2	e_3	e_1	+	−	+	mid	min	max
$5\pi/3 \sim 2\pi$	e_1	e_3	e_2	+	−	−	max	min	mid

Table 3 Output five-phase voltage relationship

Phase angle	Output phase voltages					Signs of line voltages				
θ_L	v_a	v_b	v_c	v_d	v_e	v_{ab}	v_{bc}	v_{cd}	v_{de}	v_{ea}
$0 \sim \pi/5$	v_3	v_5	v_4	v_2	v_1	+	−	−	−	+
$\pi/5 \sim 2\pi/5$	v_2	v_4	v_5	v_3	v_1	+	+	−	−	+
$2\pi/5 \sim 3\pi/5$	v_1	v_3	v_5	v_4	v_2	+	+	−	−	−
$3\pi/5 \sim 4\pi/5$	v_1	v_2	v_4	v_5	v_3	+	+	+	−	−
$4\pi/5 \sim \pi$	v_2	v_1	v_3	v_5	v_4	−	+	+	−	−
$\pi \sim 6\pi/5$	v_3	v_1	v_2	v_4	v_5	−	+	+	+	−
$6\pi/5 \sim 7\pi/5$	v_4	v_2	v_1	v_3	v_5	−	−	+	+	−
$7\pi/5 \sim 8\pi/5$	v_5	v_3	v_1	v_2	v_4	−	−	+	+	+
$8\pi/5 \sim 9\pi/5$	v_5	v_4	v_2	v_1	v_3	−	−	−	+	+
$9\pi/5 \sim 2\pi$	v_4	v_5	v_3	v_1	v_2	+	−	−	+	+

IET Power Electron., 2016, Vol. 9, Iss. 3, pp. 466–475

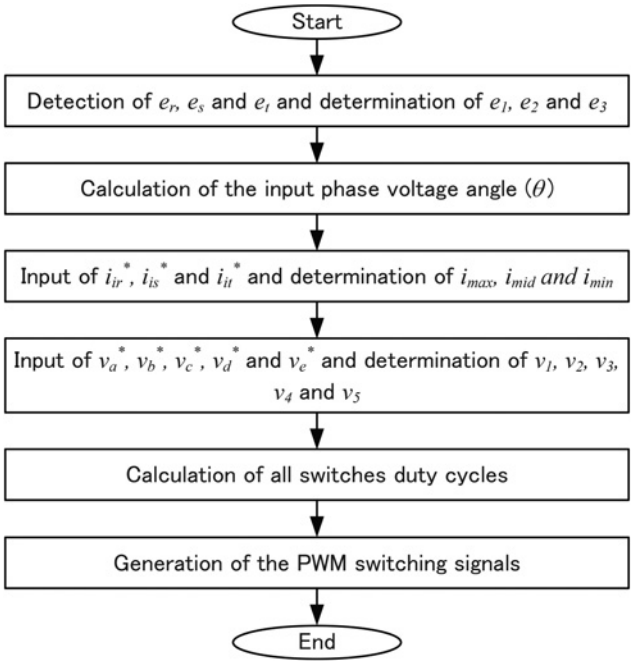

Fig. 6 *Control procedure*

5 Control procedure

Calculations of all duty cycles depend mainly on the voltage levels of the input and output voltages. The input voltages are three-phase waveforms shifted by 120° and hence there are three levels changing every 60°. The output voltages are five-phase waveforms shifted by 72° and hence there are five levels changing every 36°. The levels of the input and output voltages can be decided according to the signs of the line-to-line voltages in the input and output, as shown in Tables 2 and 3, respectively. In Table 2, the three levels of the input side are defined as maximum (e_1), middle (e_2), and minimum (e_3). Since the input currents are controlled to be in-phase with the input voltages, the levels of input currents are same as that of the input phase voltages. In Table 3, the five levels of the output side are defined as maximum (v_1), mid-high (v_2), middle (v_3), mid-low (v_4), and minimum (v_5). The duty cycles of all switches can be obtained based on the values of input currents and output phase voltages. The control procedure of the three-to-five-phase matrix converter is summarised in the flowchart shown in Fig. 6.

6 Experimental results

6.1 Experimental system configuration

A laboratory prototype of the three-to-five phase matrix converter has been carried out to investigate the validity of the proposed PWM switching technique. Fig. 7*a* shows the experimental system configuration of the three-to-five phase matrix converter. Moreover, Fig. 7*b* shows the laboratory prototype photograph. The input of the matrix converter is connected to a symmetrical three-phase voltage source through the input *LC* filter. The output of the matrix converter is connected to a balanced five-phase inductive load. Each bi-directional switch in the matrix converter has been represented by an IGBT and four diodes. A diode based clamp circuit is used between the input and output lines to protect the converter from switching transients. The dspace-1006 working in conjunction with DS5203 FPGA board has been used as a controller of the matrix converter that generates the proper PWM signals to the IGBT switches. A dead-time of 2 μs has been implemented in an external FPGA board that is programmed using VHDL to avoid the short circuit at the input side. The reference

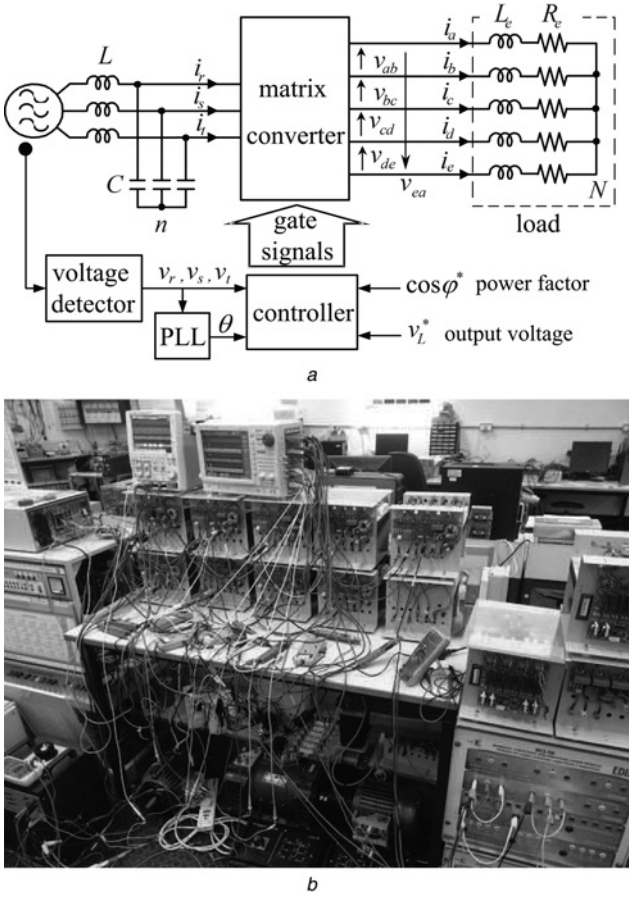

Fig. 7 *Experimental system of the three-to-five phase matrix converter*

a Configuration of the system under study
b Experimental system prototype

load voltage magnitude is set at $V_L^* = 82.3\,\text{V}$ with a reference frequency of 40 Hz. Moreover, the reference input voltage phase angle φ* is set at 0° to realise unity input power factor. The parameters of the whole system are listed in Table 4. Experimental waveforms of the converter have been measured by using Yokogawa DL750 ScopeCorder Oscilloscope.

6.2 Simulation results

The three-to-five-phase matrix converter and its proposed PWM switching technique, shown in Fig. 7*a*, have been carried out using PSIM considering the same system parameters shown in Table 4. Fig. 8 shows the simulation results including the three-phase input voltages v_r, v_s and v_t, the reference five-phase output voltages v_a^*, v_b^*, v_c^*, v_d^* and v_e^*, the actual phase (*a*) output voltage v_{an} with respect to the source voltages, the actual phase (*b*) output voltage v_{bn} with respect to the source voltages, the actual and reference line-to-line output voltages v_{ab} and v_{ab}^*, the load currents i_a, i_b, i_c, i_d and i_e, and phase (*a*) actual and reference voltages v_{aN} and v_a^*. It is clear that the load currents are five-phase waveforms with frequency of 40 Hz. Moreover, the switching in the output voltages agrees with the proposed PWM pattern shown in Fig. 4. However, there is a small distortion in the output

Table 4 System parameters

source voltage E, ω	173.2 V, $2\pi \times 50$ rad/s
input filter L, C	1.13 mH, 13.2 μF
input power-factor angle reference φ*	0 rad
load R_e, L_e	95 Ω, 193 mH
output voltage reference V_L^*, ω_L^*	82.3 V, $2\pi \times 40$ rad/s
carrier frequency $f_s (= 1/2T)$	10 kHz

currents due to the un-switched portion in each output phase voltage during its minimum level.

6.3 Experimental results

Fig. 9*a* shows the experimental waveforms of the laboratory prototype when the reference magnitude of the load line voltage is 82.3 V and the reference frequency is 40 Hz. The scope, shown in Fig. 9*a*, shows the waveforms of the source voltage and source current (v_r, i_r), load phase voltage v_{an}, line-to-line load voltage v_{ab}, and the five-phase load currents i_L. It is clear that the source voltage and current are in-phase resulting in unity input power factor. Also, the actual load line voltage magnitude is 80.1 V with frequency of 40.4 Hz and the load current is 652 mA. However, the load current has some distortion caused by the harmonic components in the load voltage due to the un-switched period during the time of minimum level.

Fig. 9*b* shows an expanded scope of the load line voltage v_{ab} with respect to the load phase voltages (v_{an} and v_{bn}) and the input three-phase voltages. It is clear that both phase voltages v_{an} and v_{bn} equal the minimum input voltage when there corresponding reference voltages are at the minimum level. Moreover, there is no direct switching between the maximum and minimum input voltages, which results in the presence of no-zero portion in the line voltage v_{ab}. This, also, agrees with the estimated switching signals of the line voltage v_{bc} shown in Fig. 4*b*.

Figs. 10*a* and *b* show the FFT harmonic spectrum of the load line voltage of the three-to-five phase matrix converter controlled by the proposed PWM technique and SVM, respectively, with reference

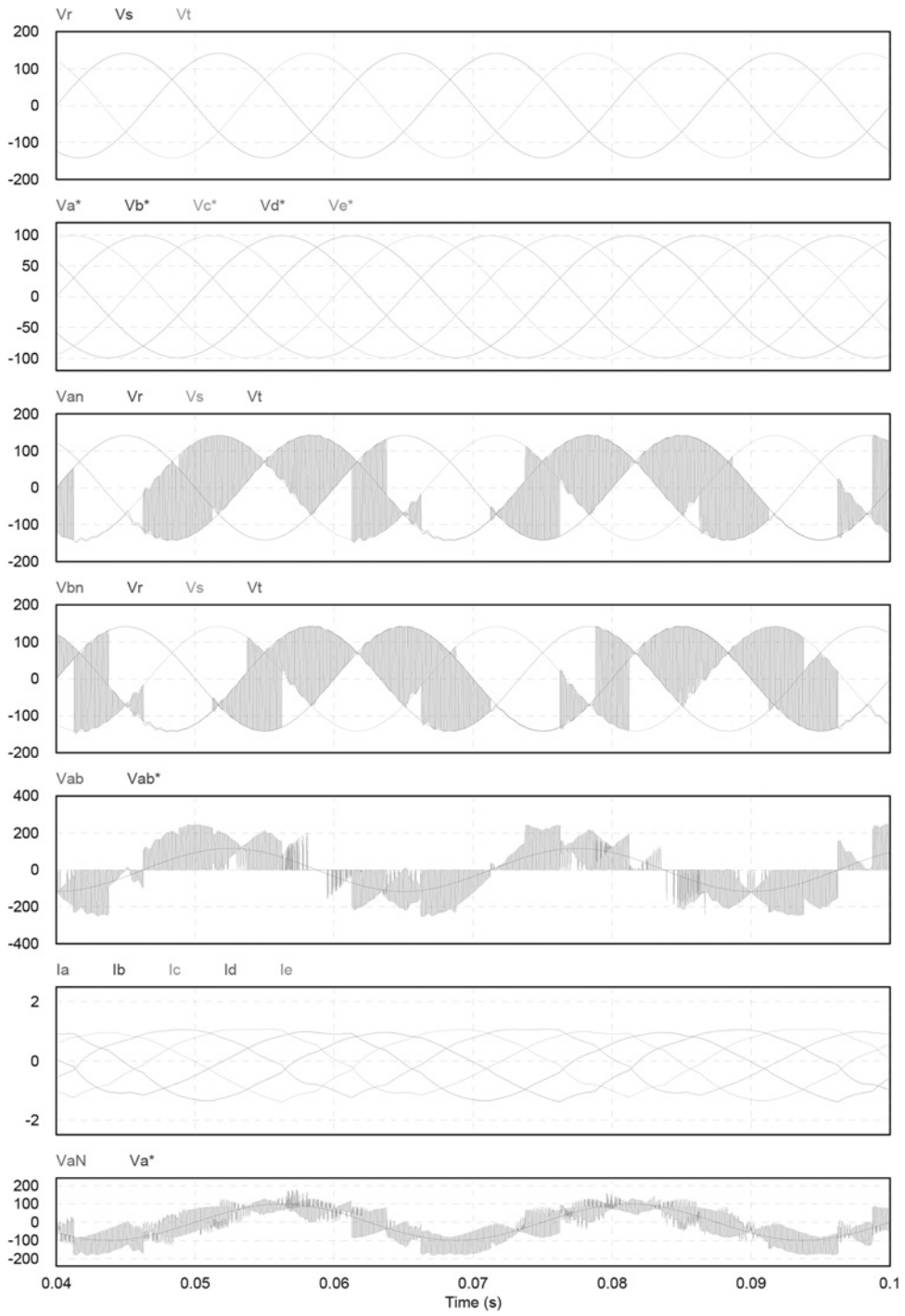

Fig. 8 *Simulation results of the system under study*

IET Power Electron., 2016, Vol. 9, Iss. 3, pp. 466–475

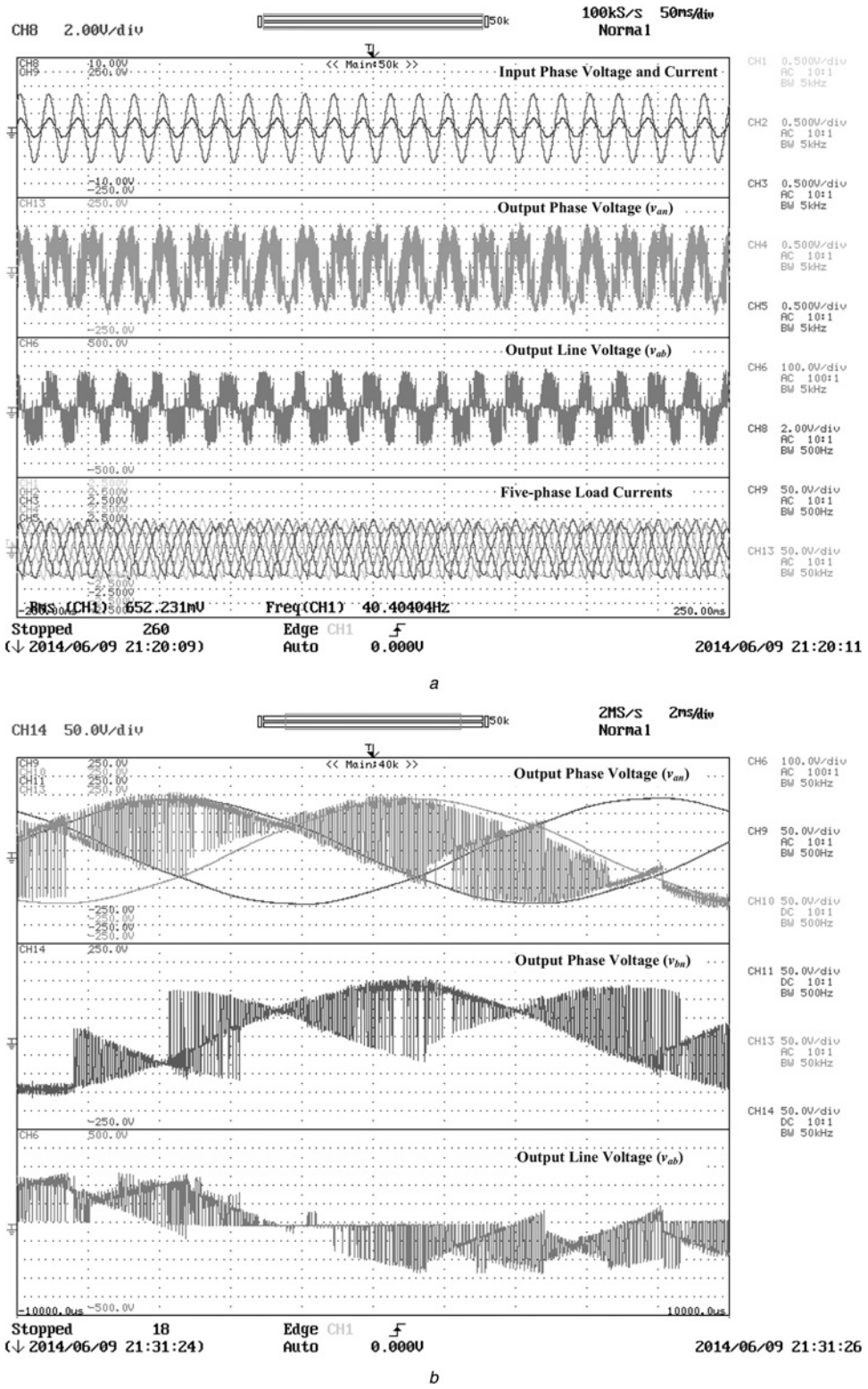

Fig. 9 *Experimental results*

a Experimental system waveforms
b Expanded scope of the input and output voltage waveforms

line voltage of 82.3 V and frequency of 40 Hz. The THD of the load line voltage in the system controlled by MVDS based five commutations is 61.1%, whereas the THD of the load line voltage is 77.14% using SVM. Fig. 11 shows the comparison between the THD of load line voltage of the three-to-five-phase matrix converter controlled by SVM and the proposed PWM technique at different modulation indexes. It is clear that the proposed MVDS provides less THD in the load line voltage at all modulation indexes.

It is clear from the simulation and experimental results that the proposed PWM technique based MVDS proves a stable operation of the three-to-five phase matrix converter. Moreover, it has the ability to control the output voltage magnitude and frequency to

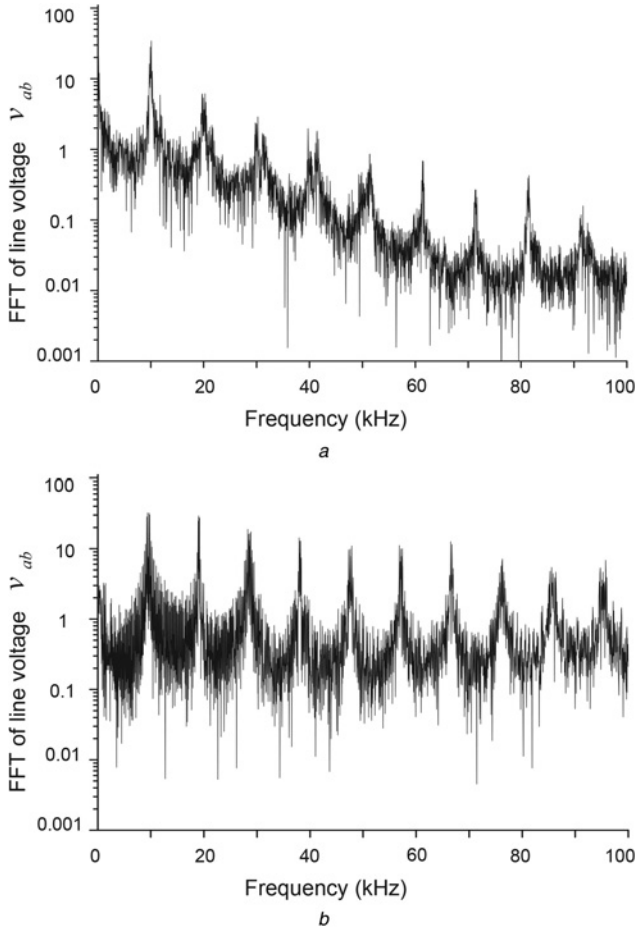

Fig. 10 *FFT harmonic spectrum of load line voltage*

a FFT harmonic spectrum of the load line voltage using MVDS
b FFT harmonic spectrum of the load line voltage using SVM

coincide with the reference values in addition to realisation of the unity input power factor.

7 Conclusion

This paper has presented a new PWM switching technique for controlling a three-to-five phase matrix converter. The proposed PWM switching technique reduces the commutation number to five in the control period. It also has the ability to realise reference load voltage up to 78.86% of the input voltage with full frequency control in addition to achieving unity input power factor. Moreover, it reduces the THD of the output line voltage and reduces the voltage stress on power switches by preventing the direct commutation or switching between maximum and minimum input voltages. Simulation and experimental results obtained from the laboratory prototype model have verified the effectiveness of the proposed PWM switching technique and the validity of the theoretical analysis.

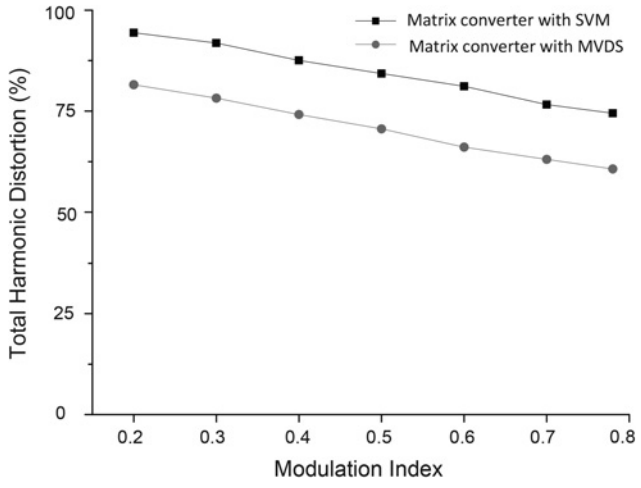

Fig. 11 *Comparison between THD of matrix converter with SVM and MVDS*

8 References

1 Rivera, M., Rojas, C., Wilson, A., *et al.*: 'Review of predictive control methods to improve the input current of an indirect matrix converter', *IET Power Electron.*, 2014, **7**, pp. 886–894
2 Lozano-Garcia, J., Ramirez, J.: 'Voltage compensator based on a direct matrix converter without energy storage', *IET Power Electron.*, 2015, **8**, (3), pp. 321–332
3 Wheeler, P., Rodriguez, J., Clare, J., *et al.*: 'Matrix converters: a technology review', *IEEE Trans. Ind. Electron.*, 2002, **49**, pp. 276–288
4 Rodriguez, J., Rivera, M., Kolar, J., *et al.*: 'A review of control and modulation methods for matrix converters', *IEEE Trans. Ind. Electron.*, 2012, **59**, pp. 58–70
5 Empringham, L., Kolar, J., Rodriguez, J., *et al.*: 'Technological issues and industrial application of matrix converters: A review', *IEEE Trans. Ind. Electron.*, 2013, **60**, pp. 4260–4271
6 Rivera, M., Rojas, C., Rodriguez, J., *et al.*: 'Methods of source current reference generation for predictive control in a direct matrix converter', *IET Power Electron.*, 2013, **6**, pp. 894–901
7 Jones, M., Levi, E.: 'A literature survey of state-of-the-art in multiphase ac drives'. in UPEC '08, Stafford-U.K., September 2002, vol. 2, pp. 505–510
8 Singh, G.K.: 'Multi-phase induction machine drive research – a survey', *Electr. Power Syst. Res.*, 2002, **61**, (2), pp. 139–147
9 Levi, E., Bojoi, R., Profumo, F., *et al.*: 'Multiphase induction motor drives – a technology status review', *IET Electr. Power Appl.*, 2007, **1**, (4), pp. 489–516
10 Levi, E., Bodo, N., Dordevic, O., *et al.*: 'Recent advances in power electronic converter control for multiphase drive systems'. 2013 IEEE Workshop on Electrical Machines Design Control and Diagnosis (WEMDCD), March 2013, pp. 158–167
11 Renukadevi, G., Rajambal, K.: 'Field programmable gate array implementation of space-vector pulse-width modulation technique for five-phase voltage source inverter', *IET Power Electron.*, 2014, **7**, pp. 376–389
12 Wheeler, P., Lie, X., Lee, M.Y., *et al.*: 'A review of multi-level matrix converter topologies'. Fourth IET Conf. on Power Electronics, Machines and Drives, 2008. PEMD 2008. April 2008, pp. 286–290
13 Govindaraju, C.: 'Efficient sequential switching hybrid modulation techniques for multiphase multilevel inverters', *IET Power Electron.*, 2011, **4**, pp. 557–569
14 Xiang-Jun, Z., Yongbing, Y., Hongtao, Z., *et al.*: 'Modelling and control of a multi-phase permanent magnet synchronous generator and efficient hybrid 3l-converters for large direct-drive wind turbines', *IET Electr. Power Appl.*, 2012, **6**, pp. 322–331
15 Goncalves de Oliveira, J., Schettino, H., Gama, V., *et al.*: 'Study on a doubly-fed flywheel machine-based driveline with an ac/dc/ac converter', *IET Electr. Syst. Transp.*, 2012, **2**, pp. 51–57
16 Rastegar Fatemi, S., Abjadi, N., Soltani, J., *et al.*: 'Speed sensorless control of a six-phase induction motor drive using backstepping control', *IET Power Electron.*, 2014, **7**, pp. 114–123
17 Salehifar, M., Salehi Arashloo, R., Moreno-Eguilaz, M., *et al.*: 'Observer-based open transistor fault diagnosis and fault-tolerant control of five-phase permanent magnet motor drive for application in electric vehicles', *IET Power Electron.*, 2015, **8**, (1), pp. 76–87
18 Iqbal, A., Ahmed, S., Abu-Rub, H.: 'Space vector pwm technique for a three-to-five-phase matrix converter', *IEEE Trans. Ind. Appl.*, 2012, **48**, pp. 697–707
19 Iqbal, A., Ahmed, S., Abu-Rub, H.: 'Pulse width modulation of direct ac-ac power converter with five-phase input and three-phase output', *Int. J. Autom. Power Eng.*, 2012, **1**, pp. 186–192
20 Iqbal, A., Salah, S., Abu-Rub, H., *et al.*: 'Simple carrier-based pwm technique for a three to quasi six-phase matrix converter', *Aust. J. Electr. Electron. Eng.*, 2013, **9**, pp. 295–304
21 Ahmed, S., Abu-Rub, H., Salam, Z., *et al.*: 'Space vector pwm technique for a novel three-to-seven phase matrix converter'. Industrial Electronics Society, IECON 2013 – 39th Annual Conf. of the IEEE, November 2013, pp. 4949–4954
22 Rahman, K., Iqbal, A., Abduallah, A., *et al.*: 'Space vector pulse width modulation scheme for three to seven phase direct matrix converter'. 2014 29th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), March 2014, pp. 595–601
23 Ahmed, S., Iqbal, A., Abu-Rub, H., *et al.*: 'Simple carrier-based pwm technique for a three-to-nine-phase direct ac-ac converter', *IEEE Trans. Ind. Electron.*, 2011, **58**, pp. 5014–5023
24 Alesina, A., Venturini, M.: 'Solid-state power conversion: A fourier analysis approach to generalized transformer synthesis', *IEEE Trans. Circuits Syst.,* 1981, **28**, pp. 319–330
25 Alesina, A., Venturini, M.: 'Intrinsic amplitude limits and optimum design of 9-switches direct pwm ac-ac converters'. 19th Annual IEEE Power Electronics Specialists Conf., 1988. PESC '88 Record. April 1988, vol. 2, pp. 1284–1291

26 Roy, G., April, G.-E.: 'Cycloconverter operation under a new scalar control algorithm'. 20th Annual IEEEPower Electronics Specialists Conf. 1989. PESC '89 Record. June 1989, vol. 1, pp. 368–375
27 Dabour, S., Rashad, E.: 'Analysis and implementation of space-vector-modulated three-phase matrix converter', *IET Power Electron.*, 2012, **5**, pp. 1374–1378
28 Iqbal, A., Levi, E., Jones, M., *et al*.: 'Generalised sinusoidal pwm with harmonic injection for multi-phase vsis'. 37th IEEE Power Electronics Specialists Conference, 2006. PESC '06. June 2006, pp. 1–7
29 Ahmed, S., Iqbal, A., Abu-Rub, H.: 'Generalized duty-ratio-based pulsewidth modulation technique for a three-to-k phase matrix converter', *IEEE Trans. Ind. Electron.*, 2011, **58**, pp. 3925–3937