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A 0.35μm Low-Noise Stable Charge Sensitive Amplifier for Silicon Detectors Applications

Folla Kamdem Jérôme[1,3], Wembe Tafo Evariste[2], Essimbi Zobo Bernard[1], Maria Liz Crespo[3], Andres Cicuttin[3], Mamun Bin Ibne Reaz[4], Mohammad Arif Sobhan Bhuiyan[5], Muhammad Enamul Hoque Chowdhury[6]

[1]University of Yaoundé I, Faculty of Science, Department of Physics, Cameroon
[2]University of Douala. Faculty of Science, Department of Physics, Cameroon
[3]International Center for Theoretical Physics (ICTP), Trieste, Italy
[4]Universiti Kebangsaan Malaysia, Centre of Advanced Electronic and Communication Engineering, Selangor, Malaysia
[5]Xiamen University Malaysia, Electrical and Electronics Engineering, Selangor, Malaysia.
[6]Qatar University, Department of Electrical Engineering, Qatar

Abstract: The Charge Sensitive Amplifier (CSA) is the key module of the front-end electronics of various types of Silicon detectors and most radiation detection systems. High gain, stability, and low input noise are the major concerns of a typical CSA circuit in order to achieve amplified susceptible input charge (current) for further processing. To design such a low-noise, stable, and low power dissipation solution, a CSA is required to be realized in a complementary metal-oxide-semiconductor (CMOS) technology with a compact design. This research reports a low-noise highly stabile CSA design for Silicon detectors applications, which has been designed and validated in TSMC 0.35 um CMOS process. In a typical CSA design, the detector capacitance and the input transistor's width are the dominant parameters for achieving low noise performance. Therefore, the Equivalent Noise Charge (ENC) with respect to those parameters has been optimized, for a range of detector capacitance from 0.2 pF – 2 pF. However, the parallel noise of the feedback was removed by adopting a voltage-controlled NMOS resistor, which in turn helped to achieve high stability of the circuit. The simulation results provided a baseline gain of 9.92 mV/fC and show that ENC was found to be 42.5 e–with 3.72 e–/pF noise slope. The Corner frequency exhibited by the CSA is 1.023 GHz and the output magnitude was controlled at -56.8 dB; it dissipates 0.23 mW with a single voltage supply of 3.3 V with an active die area of 0.0049 mm^2.

Keywords: CMOS; CSA; Front-End; Low- noise; Silicon detector

Nizkošumen stabilen ojačevalnik za silicijeve detektorje

Izvleček: Na naboj občutljiv ojačevalnik (Charge Sensitive Amplifier - CSA) je osnovni del vhodne elektronike različnih silicijevih senzorjev in večine sistemov detekcije sevanja. Veliko ojačenje, stabilnost in nizek šum so glavne zahteve tipičnih CSA vezij za doseganje zadovoljivega ojačenja naboja (toka) za nadaljnje procesiranje. Za razvoj nizko šumne, stabilne rešitve z nizko porabo mora biti CSA realiziran v kompaktni CMOS tehnologiji. V delu predstavljamo nizko šumen, stabilen CSA za silicijev detektor, ki je bil preverjen v TSMC 0.35 um CMOS tehnologiji. V tipičnem CSA sta kapacitiven detektor in vhodna širina tranzistorja glavna parametra za doseganje nizkega šuma. Ekvivalenten šumni naboj ej bil optimiran za detektiranja kapacitivnosti v razponu od 0.2 pF – 2 pF. Paralelni šum povratne vezave je bil odstranjen z napetostno krmiljenim uporom, ki je pripomogel tudi k stabilnosti vezja. Simulacije so pokazale ojačenje 9.92 mV/fC in ENC 42. 5 e– z naklonom 3.72 e–/pF. Vogalna frekvenca CSA je 1.023 GHz, in kontroliranim izhodnim signalom pri -56.8 dB. Poraba moči je 0.23 mW pri 3.3 V napajanju in aktivni površini 0.0049 mm^2.

Ključne besede: CMOS; CSA; vhod; nizek šum; silicijev detektor

** Corresponding Author's e-mail: jfollure@yahoo.fr, arifsobhan.bhuiyan@xmu.edu.my, mchowdhury@qu.edu.qa*

1 Introduction

The Modern Front-End Electronics (FEE) for High Energy Physics Experiment (HEPE) are mixed-signal circuits in which the ultimate performance is set by the analog circuit applied to Solid State Detectors. The X-Rays-Sensors interaction produces a very small current and has to be amplified in a low noise circuit before any further signal processing either on-chip or off-chip with digital techniques. In multi-detector systems, multiple channels create several complications. In order to limit the power dissipation-noise problem, the sensor should be placed adjacent to the front-end amplifier. However, this results in decreased detector resolution because of heat transfer. Moreover, the process technology utilized for designing a preamplifier determines the overall size and price of the silicon-based detector systems. When a soft X-rays strikes a semiconductor detector, charges are generated. Various types of X-ray detectors including Silicon PIN Detectors, Silicon Drift Detectors (SDDs), Silicon Strip Detector (SSD), etc. have been extensively used in order to quantify the energy and photon count of incident X-rays. This type of detectors designed with a thick Si substrate is very useful for 2-D tracking in a high multiplicity environment because of the large charge collection area along with low anode capacitance [1]. Through going X-rays, create electron-hole pairs in the depletion zone of the detector and these charges drift towards the electrodes as illustrated in Fig.1. This drift (current) creates the signal (voltage) which is very weak and must be amplified by a CSA connected to each strip.

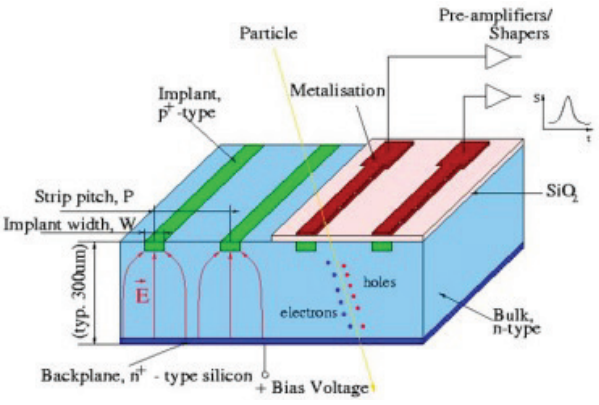

Figure 1: Principle of operation of a silicon strip detector [2].

From the signals on the individual CSA, the amplitude of the output voltage is realized. That voltage depends on the energy of the incident particles and must be measured with the highest accuracy and precision [3]. The input node voltage of the CSA increases and the voltage with the opposite polarity is generated at the output terminal simultaneously. Hence, the output potential through feedback loop forces the input potential of the CSA to become zero because of high open-loop gain as evident from Fig.2. The total amount of the current pulses is integrated on the feedback capacitor and the corresponding output is a step voltage pulse [3, 4] as described in equation (1).

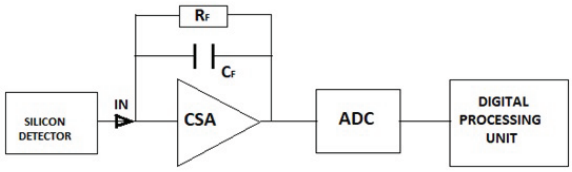

Figure 2: Silicon detector readout architecture for digital processing, the CSA is used for extracting the charge at each strip and convert it into voltage.

$$V_{CSA}(t) = \frac{1}{C_f}\int_0^T i_e(t)\,dt + V_0 \quad (1)$$

Where, VCSA(t) is the output voltage of the CSA at the time t, $i_e(t)$ is the input current injected in the detector, T is the integration period, C_f the feedback capacitor and V_0 is the offset voltage of the circuit.

As the input signals intercepted by CSA are generally very low. For a given signal source, the CSA noise performance depends on the noise created within the amplifier itself and the signal impedance seen by the amplifier input. Therefore, the CSA input stage must ensure that optimum noise matching is obtained for the given source impedance. The choice of the design parameters of the input stage of CSA influences the noise matching. So the total equivalent input noise should be kept as small as possible for a given detector capacitance up to 2pF. The main problem in the design of nuclear spectroscopy Very Large Scale Integration (VLSI) readout front ends is the implementation of low-noise; low power Charge Sensitive Amplifier (CSA). The selection of the process (CMOS or BiCMOS) determines the performance and generally the noise-related design methodology. A VLSI preamplifier costs much less than a hybrid one or a preamplifier unit [5]. CMOS exhibits several advantages over other concurrent technologies and and is preferred in VLSI circuit design [6-7]. A very popular approach in designing the VLSI CSA is the usage of an operational amplifier (Op-amp), with the R-C feedback network. Since Cdet (the detector parasitic capacitance) is quite large, about 15pF, the stability becomes a critical issue in that design [8]. For a complete validation of the CSA with CMOS technology, the overall system specifications are needed [8, 9]. In [10] H. Wang et al, proposed a CSA based Polyvinylidene Fluoride (PVDF) transducers. The circuit

works for low power dissipation and low frequency; but it iss prone to low conversion gain, high feedback capacitance that occupies more die area. A. Baschirotto et al [11], designed a CSA using a single-ended amplifier. The circuit works at high frequency and very low voltage; however, the disadvantages of that circuit are high power consumption and high Equivalent Noise Charge (ENC); furthermore, the circuit was prone to the parallel noise generated by the feedback resistor. The single-ended amplifier is a good architecture despite it is prone to both process variations and signal degradation. Indeed, the current mirrors, which generate the bias voltage for proper operation of the amplifier, contribute the common-mode noise. Thus, increasing the size of the input transistor of such an amplifier does not improve noise performance because of the bias current limitation [4]. Therefore, it is necessary to propose an optimal circuit to avoid unnecessary power dissipation and heat in closely packed pixel arrays. Secondly, the ENC should be optimized with respect to detector capacitance and the input transistor width, by performing AC and transient analysis.

In this article, a low-noise CSA designed in 0.35 µm CMOS technology process is proposed. The circuit consists of a single-ended gain block and a feedback network. The CSA bandwidth is compromised by a large detector capacitance. In order to compensate this, a common-source (CS) input design is adopted to isolate the capacitance, preventing it from affecting the bandwidth. Furthermore, CS topology is linear and power-efficient [12]. The feedback resistor stabilizes the gain-bandwidth product of the circuit. The resistor is an NMOS transistor operating as a voltage-controlled resistor; it also reduces the parallel noise contribution. The proposed circuit works with a low-energy capacitive silicon detector for X-ray detection applications.

2 Materials and methods

The CSA has been designed for a 0.35 µm TSMC process, to perform the initial conversion of current pulses into voltage pulses. Table 1 below presents the design specifications of a CSA circuit for Silicon-PIN detector applications.

Table 1: CSA specifications required for silicon detector for two vendors.

Vendor Parameters	Hamamatsu (H4083)	Amptek (A250)
Power consumption	150 mW@12V	14 mW@6 V
Count rate	2.6 MHz	2.5MHz
Detector capacitance	0 – 25 pF	0 – 250 pF
ENC (Cin = 5pF)	240 e-	76 e-
Noise slope	4 e-/pF	11.5 e-/pF
Sensitivity	22 mV/MeV (Si)	176 mV/MeV (Si)

In order to increase the gain of the CSA, we choose a three-stage configuration for the design. The single-ended configuration of the circuit in Fig. 3, is preferred to the differential one for the reduction of power consumption. The choice of the N-channel input transistor relies on the lower thermal noise compared to the P-type at high frequency, since the 1/f noise is negligible in the frequency region after 10 kHz [13, 14]; in addition, N-channel MOS, gives a lower series white noise with respect to the P-channel counterpart, because of its higher transconductance [13]. The current source at M1's drain is provided by M2, a P-channel MOSFET with smaller transconductance.

The second stage is the Miller stage. In this stage, the transistors M3 and M4 are connected in cascade whereas the transistor M5 forms the current mirror. Such a stage in the CSA incorporates a higher output resistance. The maximum signal swing must be kept limited so that all the transistors remain in the saturation region of operation, i.e., VGS> VT and VDS> VGS-VT [13]. Therefore, the bias current of M3 is kept at a specific low value (12.5 uA) in order to keep its output impedance high. Capacitor Cm provides a gain and the dominant pole in that stage; so, resistor Rm suppresses direct transmission through Cm at high frequencies.

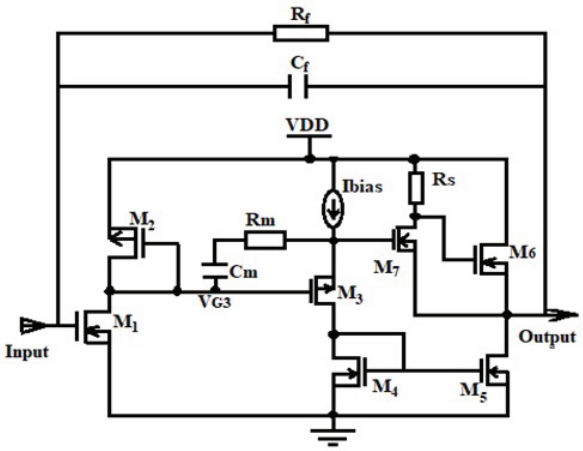

Figure 3: Schematic of the proposed structure of the CSA.

The third stage consists of an N-channel MOSFET M7 which results in a negative gain of the entire circuit so that one can apply the negative feedback. It is biased by a low current through RS. The value of Rs is set to

300 Ω so that M7 operates in the saturation region. Feedback from Vout is connected to one of the two inputs through an on-chip feedback capacitor up to 20 pF and a resistor of 30 MΩ at the top-level design. The circuit was designed with thick oxide transistors that allow a relatively high supply voltage of 3.3 V in a standard 0.35 µm CMOS technology process.

2.1 Analysis of the CSA circuit

The first stage is a cascade topology based on a common source amplifier so that the input is free from parasitic capacitance and the feedback amplifier controls the gate voltage. Therefore, the CSA input becomes a virtual ground and the detector capacitance is less significant to the CSA bandwidth.

The drains of M1 and M2 are common. When M1 is in the saturation region, we have the equation bellow:

$$V_{G3} = |V_{THP2}| + |(V_{in} - V_{THN1})| \sqrt{\frac{\mu_n}{\mu_p}\left(\frac{W_1}{L_1}\right)\left(\frac{L_2}{W_2}\right)} \quad (2)$$

When M1 enters in the triode region, the following equation (2) holds

$$\mu_n\left(\frac{W_1}{L_1}\right)\left[2\left(V_{in} - V_{THN1}\right)V_{G3} - {V_{G3}}^2\right] = \mu_p\left(\frac{W_2}{L_2}\right)\left(V_{G3} - V_{THP2}\right)^2 \quad (3)$$

with this topology, the dopants are not concentrated near the surface, so their effect is less than expected. Therefore, the voltage at the gates of M2 and M3 should depend on Rm and the reference current of M2.

In the second stage of CSA circuit, transistor M3 is in the saturation region and its drain-source current is defined by the formula:

$$I_x = \frac{1}{2} C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)\left(V_{G3} - V_{THP3}\right)^2 \quad (4)$$

Transistor M3 remains in the saturation region until the device enters the triode region where

$$V_{G3} = V_{THP3} + \sqrt{\frac{2I_{bias} + 2V_{THP3}/R_m}{C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)}} \quad (5)$$

As the whole circuit is designed to work in the saturation region, equations (2) and (5) involve:

$$I_{bias} = C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)\left[V_{THP2} - V_{THP3} + \left|\left(V_{in} - V_{THN1}\right)\right|\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{L_2}{W_2}\right)}\right]^2 - \frac{V_{THP3}}{R_m} \quad (6)$$

The biasing current helps to deplete a larger portion of the substrate and the p-well. That current depends on both the geometric and threshold voltage of transistors M1, M2 and M3. Those parameters are influenced by the mismatch of the circuit. At threshold voltage of the transistor, the instantaneous current flowing from source to drain gets a sudden boost and the additional gate voltage rise causes an exponential increase of the current. The threshold voltage of a transistor is not constant and depends on physical, electrical, and environmental factors. It has two parts: ΔV_{TH0} that is supposed to be persistent for a given technology, device, etc. [15] and ΔV_{TH} that depends on operational parameters. The V_{TH} can be expressed in the equation (6) as

$$V_{TH} = V_{TH0} + \Delta V_{TH} \quad (7)$$

Assuming V_{TH0} constant for each transistor and ΔV_{TH} identical for each type of transistor, the final expression of Ibias can be expressed as follows:

$$I_{bias} = C_{ox}\mu_n\left(\frac{W_1 \times W_3}{L_3 \times W_2}\right)\left(V_{GS1} - V_{THN0} - \Delta V_{THN0}\right)^2 - \frac{V_{THP0}}{R_m} - \frac{\Delta V_{THP}}{R_m} \quad (8)$$

Fluctuations in ΔVTH occur mainly because of temperature and voltage variations which initiate effects such as Drain Induced Barrier Lowering (DIBL), short channel effects, narrow width effect, back bias dependent threshold shift, hot carrier effect, etc. So, the biasing current as a function of the threshold voltage was computed for the limited amount of current for the circuit [15] [16].

2.1 Noise optimization of the CSA circuit

One of the primary objectives of a typical CSA design is the minimization of the ENC and this necessitates a precise input stage design. In general, the noise associated with the drain current of the input device is the vital part of the ultra-low-noise design, [17]. Past research on ENC noise minimization in the CSA focused on the geometric characteristics (W and L) or the transconductance (gm) of the input transistor. However, the leakage current is a crucial parameter of the detector which seriously affects the resolution and reliability of the detector. It is related to many factors, such as the quality of silicon, process flow, temperature, etc. which is difficult to accurately express by analytical formula. Gate-controlled diodes have been frequently used to characterize leakage current components and extract minority carrier lifetime [16] [24]. Some detailed leakage current analyses with gate-controlled diodes have been performed in regular thickness wafer for a radiation detector [16]. This research, presents the ENC as a function of the detector capacitor and the feedback for a fixed value of W and L, according to the adopted

CMOS process. The leakage current is 10nA. The different contributions are evaluated as follows:

The most prominent thermal noise contribution can be calculated as:

$$ENC_{th}^{\ 2} = 4K_B Tn\gamma\alpha_n \frac{\left(C_{\det} + C_f + C_g\right)^2}{g_m C_g} \frac{N_{th}}{\tau_p} \quad (9)$$

In which KB is the Boltzmann constant, T is the room temperature, η is the body factor, γ is the inversion factor, αn the excess noise factor, Nth is the shaper noise index for the thermal noise, τp is the peaking time, Cdet the detector capacitance, Cf the feedback capacitance, Cg the gate capacitance and gm the input MOSFET transconductance.

The flicker noise or the noise due to 1/f is expressed as:

$$ENC_f^{\ 2} = K_f \frac{\left(C_{\det} + C_f + C_g\right)^2}{C_g} N_f \quad (10)$$

Where Kf is the flicker noise coefficient and Nf the shaper noise index for flicker noise. Considering the fact that, $g_m = \sqrt{2\mu \frac{C_g I_D}{L^2}}$ with Cg = Cox WL [12], equations (9) and (10) are respectively written as:

$$ENC_{th}^{\ 2} = 4K_B Tn\gamma\alpha_n \frac{\left(C_{\det} + C_f + C_{ox}WL\right)^2 L}{\sqrt{2\mu I_D}\left(C_{ox}WL\right)^{\frac{3}{2}}} \frac{N_{th}}{\tau_p} \quad (11)$$

$$ENC_f^{\ 2} = K_f \frac{\left(C_{\det} + C_f + C_{ox}WL\right)^2}{C_{ox}WL} N_f \quad (12)$$

The white parallel noise contribution to the MOSFET gate current due to the detector leakage current, can be written as:

$$ENC_i^{\ 2} = 2qI_{leak} N_i \tau_p \quad (13)$$

Where, Ileak is the leakage current associated with shot noise, and Ni is the shaper noise index for the shot noise. This term doesn't depends on W and ID.

Different components of the ENC were optimized with respect W and ID first, and the with respect to Cg. A first-order (n = 1) shaper has been used. Therefore the thermal noise is optimal if

$$\frac{\partial ENC_{th}^2}{\partial W} = 0 \quad (14)$$

Equation (14) is satisfied. The solution of that equation (14) is Wth = ((Cdet + Cf)/3CoxL), where, Wth = 42 µm for Cdet=Cf = 0.2 pF. Similarly, the flicker noise is optimal when equation (15) is satisfied.

$$\frac{\partial ENC_f^2}{\partial W} = 0 \quad (15)$$

The solution of that equation (15) is: Wf= 3 Wth with (Wf=126 µm).

The ENC as a function of ID and W is computed for both the thermal and the flicker noise. In this study, the lowest width (Wth= 42 µm) has been considered for achieving a minimal thermal noise contribution. The flicker (1/f) noise of the drain current of the preamplifier is associated with the input transistor. This is because of the generation and recombination of carriers in the two depleted regions from impurity atoms and lattice defects [16]. The instability of the drain current (ID) is established by the variation of charge in the depletion region, which constitutes the channel width. Therefore, an optimal width involves an optimal drain current of 70µA. If the trapping and releasing of carriers were purely random, the noise spectrum would be uniform. The ENC of the whole CSA circuit is calculated by adding the contributions of thermal noise, flicker noise and the shot noise [14, 17, 18]. In order to make noise as small as possible, Kf is needs to be as small as possible. Its value depends on the adopted technology process as well. Therefore, the total ENC can be expressed as:

$$ENC_{total}^2 = ENC_{th}^{\ 2} + ENC_f^{\ 2} + ENC_i^{\ 2} \quad (16)$$

$$ENC_{total}^2 = 4K_f N_f (C_f + C_{\det}) + \\ + \frac{64}{3} K_B Tn\gamma\alpha_n \frac{N_{th}}{\tau_p} \frac{\sqrt{C_{\det} + C_f}}{\sqrt{6\mu_n I_D}} + 2qI_{leak} N_i \tau_p \quad (17)$$

Where, ENC_{th}, ENC_f and ENC_i are the thermal flicker and shot noise components respectively. Mostly, ENC_{th} is the dominant part of overall ENC noise. Equation (14) is computed and the ENC could be represented by the following expression.

$$ENC = 42.5e^- + 3.72e^- / pF \quad (18)$$

Input transistor capacitance, Cin, contributes to the total capacitance of the input of the preamplifier, Ctot, which affects the series white noise and the 1/f noise contribution to the total noise. If the width of the gate-channel is reduced, Cin as well as the transconductance (gm) decrease, which results in higher series white noise spectral density. In order for the transconduct-

ance to be as large as possible, a relatively large width transistor is preferred [15, 18]. Moreover, if the detector capacitance dominates over the transistor capacitance, a large Cin value results in a small noise increment. However, such a Cin can be balanced by matching it to the detector capacitance. Table 2 and Table 3 illustrate the constant parameters used for this design and the transistor sizing for the proposed CSA design.

Table 2: Main constant parameters.

Symbol	Quantity	Values
n	body factor	1.5
α_n	excess noise factor	0.93
γ	inversion factor	0.53
N_f	shaper noise index for flicker noise	3.69
N_{th}	shaper noise index the thermal noise	0.92
K_f	flicker noise coefficient	$8.5.10^{-25}C^2m^{-2}$
g_m	input transistor transconductance	614 µS

Table 3: Transistor parameters (W/L).

Transistors	W/L (µm)
M1	42/0.35
M2	0.84/0.35
M3	18/0.35
M4	18/0.35
M5	12/0.35
M6	12/0.35
M7	9/0.35

3 Results and discussions

The proposed CSA circuit performance was verified using LTspice simulator and the layout was implemented in 0.35 µm CMOS technology process from TSMC, using Electric VLSI, which is an open source tool for integrated circuit design. Fig. 4 shows the gain of the proposed CSA. It is controlled by the Ibias value for a feedback loop of Rf = 150 kΩ and Cf = 2 pF. Frequency domain analysis was performed from 1Hz to 10 GHz. The bias current is adjusted by changing the value of the external resistor allowing changing the transconductance as represented in equation (7). The gain (absolute value) varied from 40.6 dB to 53.8 dB. The highest bandwidth of the amplifier is achieved for 12.5µA bias current, and is equal to 1.023 GHz. The optimization of the bias current of the second stage is very important for stabilizing the gain-bandwidth product and maintaining signal integrity [19]. The capacitor of the detector was set to 1 pF and the parasitic capacitance of the input transistor is around 20 fF. So, total input capacitance was 1.02 pF.

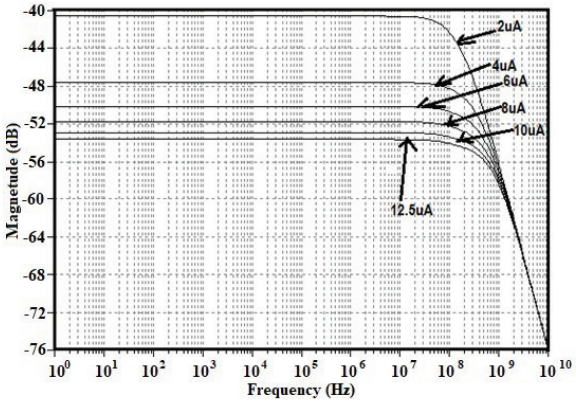

Figure 4: Influence of Ibias on the gain.

One of the most critical points in CSA is the loop gain stability, which is determined by its feedback capacitance. Nevertheless, a resistor has a parasitic capacitance and a capacitance has a parasitic resistance. Thus, an RC feedback network (Rf-Cf) models the feedback circuit. Loop-gain stability has been evaluated during the charge vs voltage conversion when Rf-Cf is bypassed [9]. The Opamp equivalent load capacitors are also taken into consideration by varying Cf. For achieving the highest stability of the circuit, the gain is adjusted by the Rf-Cf sizing. Rf was implemented by associating the drain-source resistance of a N-channel MOSFET device biased to be in the triode strong inversion region. Under this condition, the parallel noise was eliminated; the circuit is therefore stable and continuously sensitive and can be maintained in this condition without adjustment for spectroscopy purpose [10, 22, 23 and 24]. Thus, with that technique, we achieved a feedback resistance of 30 MΩ with a W/L = 25. The magnitude of the gain is therefore represented for each parameter of the feedback network. Thus, for Rf = 150 kΩ, Cf is varied from 2 pF to 20 pF. Fig.5 shows the variations of the gain for different values of Cf. For frequencies lower than 100 kHz, the parasitic capacitance of the input transistor and the resistive feedback affect the gain of the CSA and its bandwidth. The closed loop bandwidth achieved in this topology is 459.6 MHz. The circuit is immune to those parasitic effects for frequencies greater than 100 kHz. The same analysis could be applied to Fig. 6, where a MOSFET controller resistor, sized to be 150 kΩ, substituted the resistive feedback. The gain is immune to the resistive feedback and the parasitic capacitance. These results confirm the stability of the circuit with a feedback MOSFET resistor. A bandwidth of 1.023 GHz can be achieved without compromising the stability of the circuit (with output magnitude of -56.8 dB). By adjusting Ibias as shown in

Fig. 4, the bandwidth could be increased to more than 1.9 GHz.

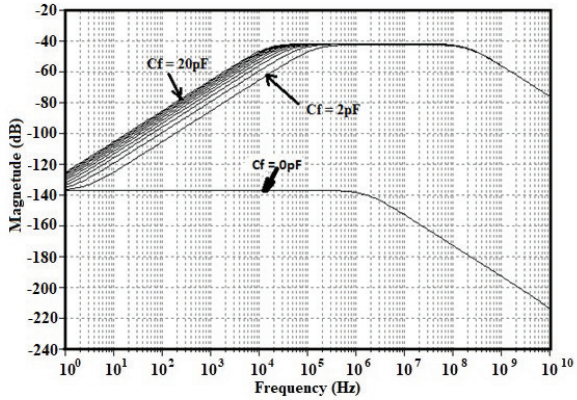

Figure 5: Influence of Cf on the gain with Rf feedback.

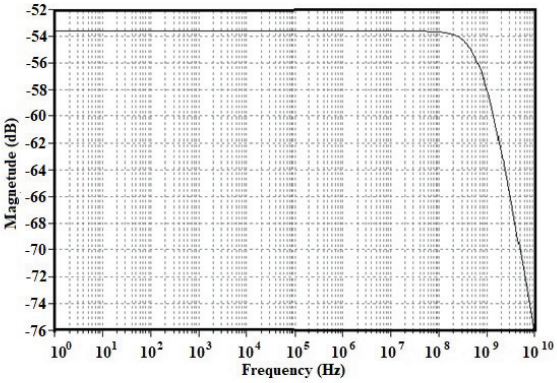

Figure 6: Influence of Cf on the gain using a MOSFET equivalent of Rf.

In Fig. 7 the Input-referred-noise (IRN) is plotted in the frequency range of 1 GHz to 10 GHz. The IRN (noise density) value extracted is 2.38 nV/√Hz. Furthermore, while designing a recording analog front-end (AFE), a lower IRN ensures the better signal quality and low power consumption will extend the lifetime of the device [19]. However, in the CSA, the parameter that embodies the noise performance is the ENC (Equivalent-Noise-Charge), namely the input charge necessary to get at the output a signal equal to noise. Its calculus was based on this intrinsic definition, neglecting the standard calculus depending on the post-CSA circuit, not present in this design [10]. Therefore, the ENC was computed and extracted based on equation (14); it presents a constant value of 42.5 e- for a detector capacitance of 0pF and noise performance increases with a slope of 3.72 e-/pF. For exhibiting the dominant component of the input noise, the ENC as a function of ID and W for the thermal component is computed in Fig. 8, and compared to the flicker noise component, which depends on W as shown in Fig. 8 and Fig. 9. In Fig. 8, when increasing the current in the input transistor, its thermal noise decreases but the bandwidth over which the thermal noise is integrated increases by the same amount; both effects cancel each other out. It can be depicted in Fig.8 and Fig .9 that the most dominant component of the ENC noise is the thermal noise component. Thus, if the device operates in a low count rate environment, substantial reductions in power consumption can be obtained with little or no noise penalty by reducing the bias current of the input transistor provided a good separation between the preamplifier rise and fall time is ensured [25].

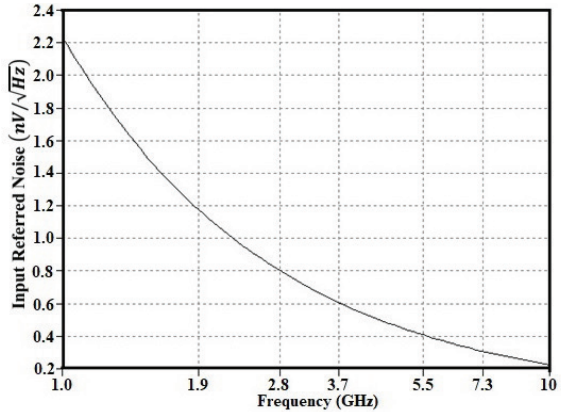

Figure 7: CSA Input-Referred Noise.

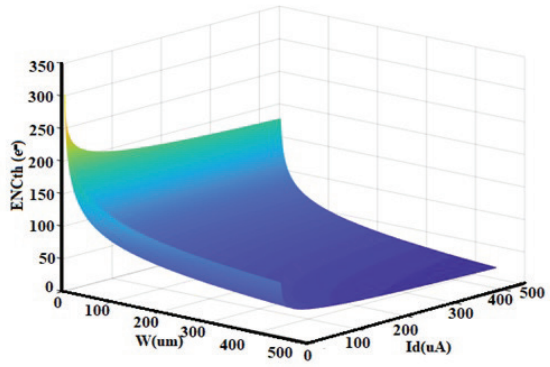

Figure 8: ENCth as a function of W and Id.

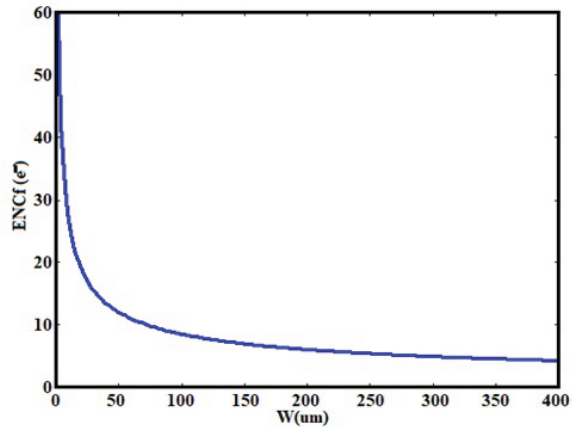

Figure 9: ENCf as a function of W.

The transient response of CSA is shown in Fig.10 and Fig.11. A current pulse with an amplitude of 33 µA and width of 1ns (206250 electrons) is injected into the detector. The output of CSA achieves a peak of 330mV and decreases thereafter because of the feedback action. For a detector capacitor of 0.2 pF, the bias current of M3 is varied and the results are shown in Fig.10. It is evident that Ibias helps to keep a lower offset and better resolution of the circuit. The same analysis is made by fixing the bias current at 12.5 µA and varying the detector capacitor from 0.2 pF to 2 pF on Fig.11. The highest amplitude (1.23 V) is obtained with 0.2 pF detector capacitance; while the highest capacitor (2 pF) generates saturation of the CSA. The output voltage is distorted and the energy information is lost which results in a circuit with low resolution. [5][26]. The fall time of the signal is about 300ns (determined by Cf and Rf).

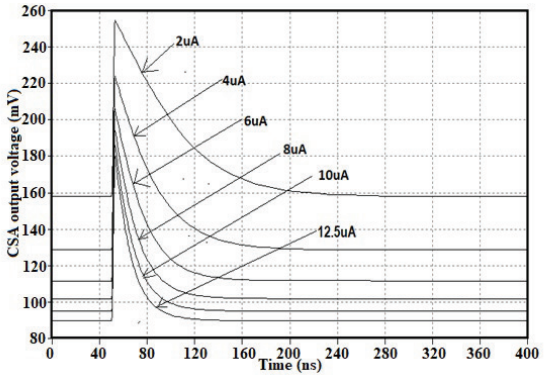

Figure 10: Ibias effect on CSA output voltage.

The amplitude of the signal charge obtained with a semiconductor detector is determined by the input particle energy such as soft X-rays and gamma rays and by the material of the semiconductor [14]. For Si-PIN diodes, the capacitance scales with area, so large area detectors exhibit more noise [21]. For SDDs, the capacitance is much lower and nearly independent of area. This noise is weakly dependent on temperature and leakage current. Since leakage current increases exponentially with temperature, reducing temperature helps dramatically [1].

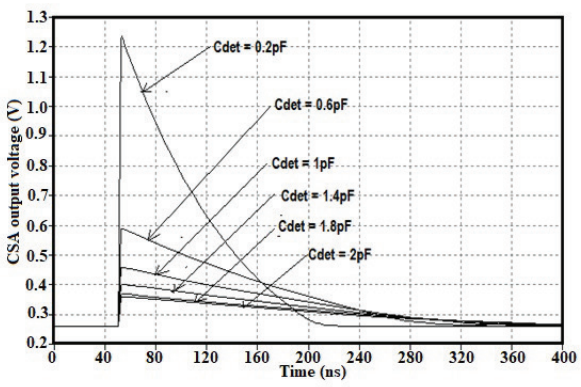

Figure 11: Cdet effect on CSA output voltage.

The total core layout area occupied by the proposed CSA is (88x55.7) µm2 as shown in Fig. 12. Parasitic extraction was used to extract the netlist with parasitic. The voltage supply is 3.3 V; the total power consumption is about 0.23 mW for the whole circuit. In this research, the gain-bandwidth product of the circuit was stabilized by means of a high-frequency feedback loop, which operates according to the voltage controlled NMOS resistor (Rf) technique [10] with resistance between 30 kΩ and 30 MΩ and a capacitance of 2 pF. The response of the circuit to different input charges results in good amplification. The gain linearity of the specific preamplifier implementation was extracted and the circuit energy response is shown on Fig. 13. The non-linearity of the CSA's gain shown on Fig. 14 (within 4.6% up to Qin=420 fC, and within 0.8% up to 300 fC) is mostly due to the second order effect of the dependence of Rf (MOSFET) on the input charge. The single MOSFET feedback network provides minimum thermal noise and high linearity, but requires baseline stabilization, and can be realized in multiple stages. [22]. The absolute value of the conversion gain is 9.92mV/fC.

Fig. 15 shows the Monte-Carlo results of the proposed circuit for 500 runs. The output signal and the histogram of the conversion gain of the circuit are shown for 10 fC injected at the input of the detector. The output signal varies from 100mV to 50 mV due to the variations of the different parameters of the circuits with the tolerance of 10%. In fact, the process variation of Ibias increases the dc-gain of the core amplifier as explained in the previous sections. The highest sensitivity of the design is then presented on Fig.15a, for a weak amount of injected charge (10fC); the circuit achieved an amplitude of 100mV. However, the histogram of conversion gain observed on Fig.15b shows a mean value of 9.79 mV/fC, and a standard deviation of 1.64 mV/fC. This indicates that the results obtained with Monte-Carlo models do not differ significantly for 500 runs and the CSA performance is quite stable and reliable.

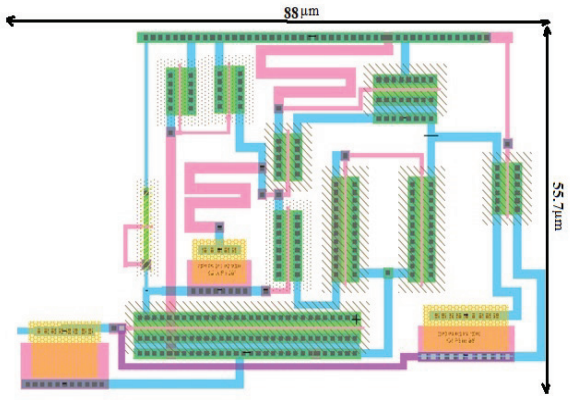

Figure 12: The core layout of the CSA circuit.

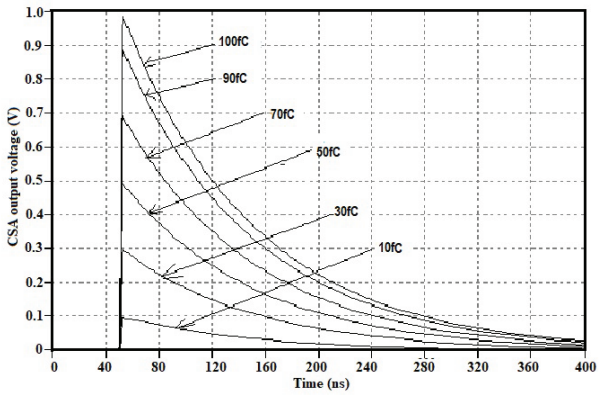

Figure 13: CSA output voltage for different input charge

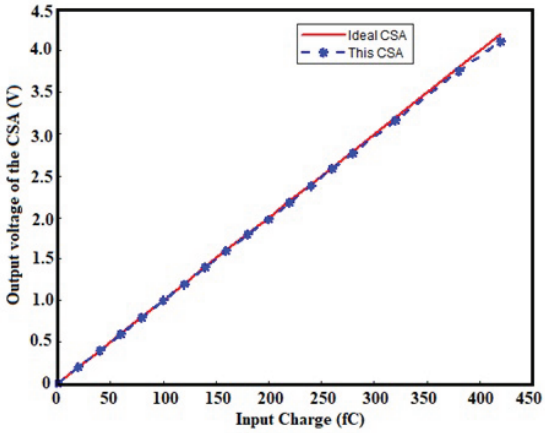

Figure 14: Output voltage vs input charge of the CSA circuit

As a summary, in Table 4 the overall features of the CSA circuit are shown. The effort in reducing power consumption, ENC and active die area of the chip comes in the parallel with similar application design present in literature [5, 8, 10, 11, 14, 21, 26]. Considering the significant difference in the input capacitance, the results are encouraging. Therefore, the preamplifier performance is in agreement with the initial specifications

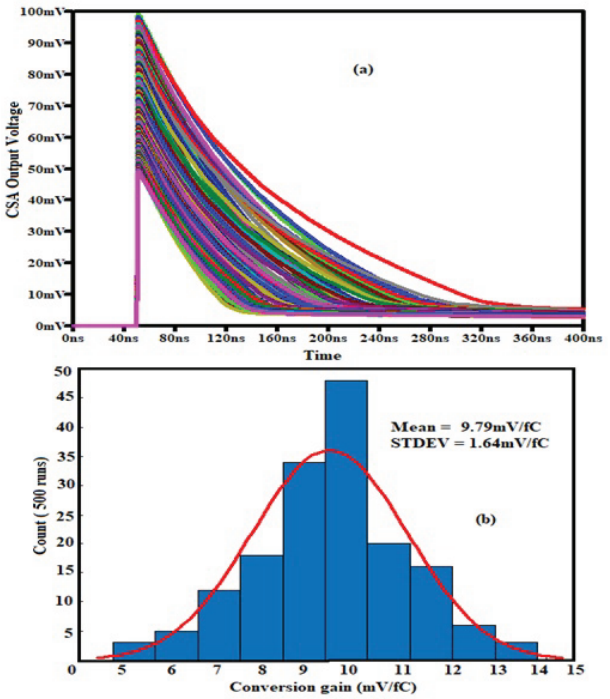

Figure 15: Post-layout Monte-Carlo simulation results (a) Output voltage (b) Conversion gain.

required. On the one hand, the design of the input and feedback transistors allowed us to achieve high linearity, wide bandwidth and sufficient low noise to ensure the good resolution of the below-threshold part of the spectrum in [26]. On the other hand, the optimization of Ibias helps to control the dc gain of the circuit and avoid saturation of the device. Operational Amplifier stability has been guaranteed with a 53.8 dB minimum dc-gain.

4 Conclusions

In this research, a 0.35 µm low-noise stable CSA circuit has been designed for Silicon detector applications.

Table 4: CSA performance summery and comparison.

Parameter	This Work	[5]	[8]	[17]	[21]	[10]
CMOS Technology	0.35 µm	0.35 µm	0.13 µm	0.13 µm	0.35 µm	0.18 µm
Power Supply	3.3 V	1.65 V	1.8 V	1.2 V	3.3 V	1.8 V
Power Consumption	0.23 mW	0.165 mW	1.1 mW	4.8 mW	--	2.1 µW
Input Parasitic Capacitance	0.2 pF – 2 pF	2 pF	15 pF	5 pF	10 pF	--
ENC	42.5 e + 3.72 e/pF	254 e- +13.5 e/pF	418 e	600 e + 100 e/pF	650 e	--
Amplifier Gain	9.92 mV/fC	2.81 mV/fC	0.5 mV/fC	10 mV/fC	15 mV/fC	0.8 µV/fC
Active area (mm^2)	0.0049	0.004212	--	0.7225	0.75	0.038
Input Dynamic Range	0– 480 fC	0 – 120 fC	--	0 – 60 fC	80 fC	150 pC – 450 pC

As per CSA, design requirements, the detector capacitance and the input stage transistor aspect ratio have been optimized in order to achieve the possible low noise and high gain performance. Moreover, adopting NMOS feedback voltage-controlled resistor technique, parallel noise that could be generated by the feedback resistance is removed which in turn ensures high stability of the design. This CSA operates at the amplification of 53.8 dB and works up to 1.023 GHz. It achieved a Charge-Voltage Conversion Factor of 9.92 mV/fC, which is compatible with the state-of-the-art. With a supply voltage of 3.3 V, it dissipates very low power of 0.23 mW. Furthermore, the proposed CSA active die area is only 0.0049 mm2. The satisfactory linearity of this circuit could be used to improve the energy resolution of X-ray radiation detection systems. The achieved results make the proposed CSA a compatible candidate for multi-channel front-end readout ASIC for Silicon detectors applications.

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6 Conflict of Interest

The authors declare no conflict of interest. Besides, the founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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