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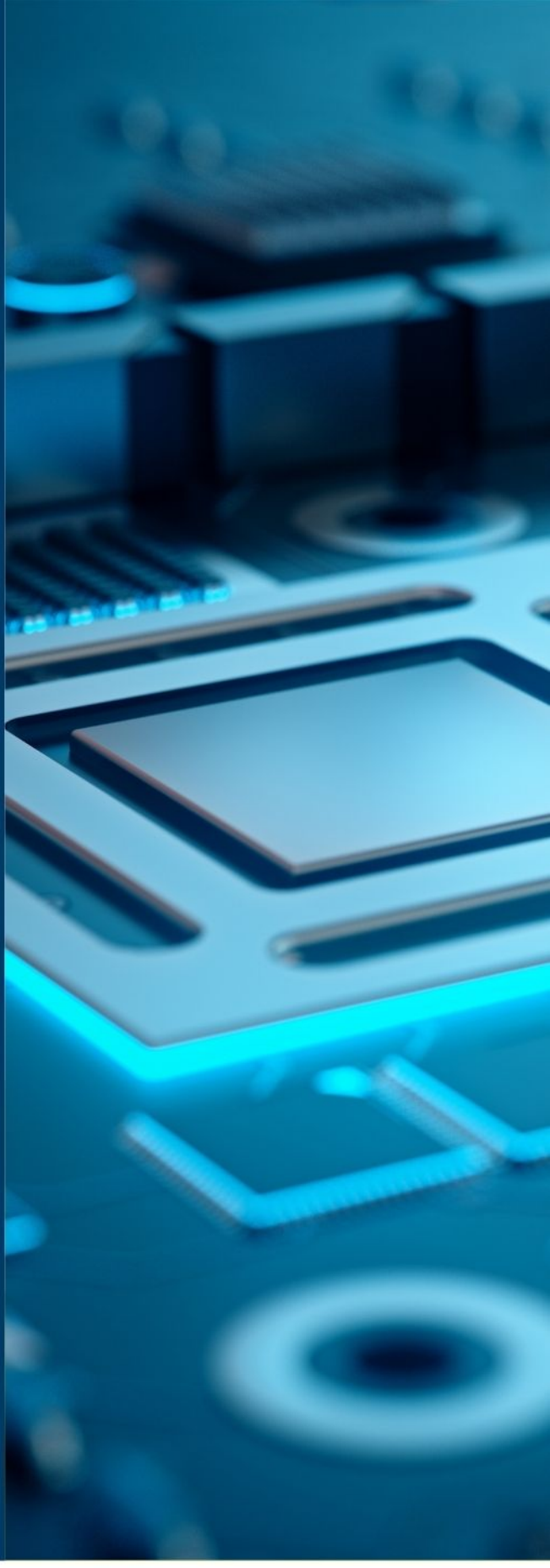

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ORIGINAL RESEARCH

Ultra high gain step up DC/DC converter based on switched inductor and improved voltage lift technique for high-voltage applications

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Abstract

Voltage lift is a well-known technique to improve the voltage gain of the converter. A combination of switched inductor and the conventional voltage lift technique can be used to achieve high gain, but the semiconductor's stress is still high. An improved voltage lift technique by employing an extra diode and capacitor and a switched inductor is proposed, which significantly increases the voltage boosting factor and reduces the voltage stress of semiconductor devices. The proposed converter is transformerless and non-isolated in nature. The proposed topology has a continuous input source current and has a common connection between the source and the load. The converter is controlled by a single switch, making it simple to use. The steady-state relations are drawn out in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The effect of the unequal inductance on the voltage gain is carried out in detail. The improved voltage lift technique can develop the *n*-stage converter to improve voltage gain further and reduce stress on semiconductors. The proposed topology is compared with the recent converters, and the effect of the non-idealities on the voltage gain and losses occurring in the components is discussed in detail. A hardware prototype with a rating of 20V/300V, 250 W is built to test the suggested topology's performance and theoretical analysis. At a 20-V input, the highest efficiency was measured to be 95.8%.

1 | INTRODUCTION

Due to greenhouse gas emissions, the globe is experiencing climate change and global warming issues. Compared to fossil fuels, renewable energy sources such as solar photovoltaic (PV), wind energy, and fuel cells are the fastest growing, cheapest and have the least environmental impact. One of the major drawbacks of these sources is the low voltage generated (12–60 V). The use of DC/DC converters to step up voltage (300–400 V) for grid use is required for the implementation of various renewable energy sources. Several battery-powered applications, such as high-intensity discharge (HID) lamp ballasts used in automotive headlights, data centres, and telecommunications systems using 400 V DC buses [1–2], and in railway system a fuel cell battery hybrid tramway use step up dc/dc converters to regulate dc traction bus voltage (700–800 V), require large step up ratios [2].

The traditional boost converter (TBC) is a type of DC/DC converter that boosts the output voltage. TBC has limitations in reality because, in order to attain high gain, it must run at a high duty ratio, but due to parasitic resistance, component voltage drop, and the diode reverse recovery, the performance is worst. Despite its simple construction and low cost, they are not exploited for energy transmission with high voltage gain [1–2]. The two primary types of converters are isolated and non-isolated [1–11]. Forward, flyback, push–pull, half-bridge, and full-bridge isolated converters use a transformer to isolate the source and the load. A significant voltage gain may be attained by increasing the number of turns. The converter is huge and expensive due to the use of a high-frequency transformer. Non-isolated converters, such as buck, boost, buck-boost, SEPIC, and Cuk, lack high-frequency transformers, resulting in smaller sizes, lower costs, and higher efficiency [2]. Coupled and non-coupled non-isolated converters are available. The coupled

inductor technology can also be used to increase the voltage gain of the converter by increasing the number of turns in a coupled inductor, but it may cause a voltage spike across the power switch. Furthermore, the problem of leaking inductance losses reduces efficiency. As a result, an additional snubber circuit is required, making the circuit more complicated. In paper [3], a coupled inductor and a switching capacitor are used to achieve high voltage gain. In [4], a three-winding coupled inductor with a voltage multiplier is employed to achieve high voltage gain. The leakage inductance is low because there are fewer turns [4]. Although the non-coupled inductor has a structure similar to that of a standard boost converter, it is related to some boosting approaches and does not have the problem of leaking inductance. One option to enhance the voltage gain of the converter is to cascade the converters, although this reduces the converter's efficiency dramatically. In article [5] a new cascade approach is used to obtain high gain, lower switch voltage stress, and lower conduction losses. Switched inductor [6–11], switched capacitor [12–15], multilevel and interleaved are some of the well-known and accepted approaches. The high voltage is obtained by combining a switched inductor with a switched capacitor cell, as shown in [12], although the converter is only suited for floating loads.

In terms of semiconductor voltage stress and power density, another boosting technology, such as high step-up converters [13–15] using switched inductor with capacitor (SC) voltage multiplier, outperforms semiconductor voltage stress and power density. The input source charges the capacitor in the circuit when the switch is on, and the stored energy is discharged when the switch is off, resulting in a greatly increased voltage conversion ratio. The suggested converter in the literature [16–17] does not work across a large duty cycle range. The inductor is substituted by an impedance network in such converters, which are categorized as quasi-z-source or z-source converters. A transformerless active switching inductance (ASL) with a simple structure is shown in [18], along with a low voltage stress on the active switch. Converters are provided in [19] to boost the voltage gain and lower the voltage stress of hybrid switching reactors. As illustrated in [19], an active LC network is implemented to alleviate the ASL network's disadvantage. Two switches are used in these converters, although the converter in [20] does not have a common ground structure. The proposed converter has a common connection between the input source and the output loads. A new impedance network is introduced in [21], and the converter can extend the impedance network in *n*-stages, but the converter's efficiency suffers as a result.

The step-up converter's continuous input current makes it suited for renewable energy applications. A redesigned SEPIC converter with high gain and constant input current is reported in the paper [22]. Another modified SEPIC structure is presented in [23] by adding four elements. In [24], a buck-boost converter with a continuous input and output port with a higher conversion rate is proposed. Paper [25] presents another buck-boost architecture, although its uses are limited because of a discontinuous input current. A switched inductor voltage multiplier with a capacitor is utilized in a traditional quadratic boost converter (TQBC) in [26] to obtain twofold quadratic gain, but the converter uses three inductors, rather than two as the suggested converter in this manuscript. The voltage stress of the converter shown in [27] is the same as the output voltage, which is a major drawback of the converter.

On the other hand, the converters indicated above only assess the voltage stress on the switch when it is turned off. Furthermore, the voltage stress on power diodes must not be overlooked. Because the voltage stress on the output diodes in the converters outlined above is equivalent to the output voltage, a high-rated power diode should be utilized at the output. In comparison to these converters with minimal voltage stress on the output power diode, the suggested converter has several advantages.

One of the well-known techniques is the voltage lift (VL) technique used to design electronic circuits. The voltage is boosted using a diode and a capacitor across inductors [28–33]. Examples of voltage lift techniques are self-lift, re-lift, triple-lift, and quadruple-lift boost converters [28]. A similar concept of voltage lift technique is used in [29] across both the inductors of the TQBC. This enhances the voltage gain and reduces the voltage stress on power devices. An active switched inductor LC (ASLC)-based dc/dc converter that uses the voltage lift technique is reported in the literature [30–31], but the converter is suitable for floating loads only. Another converter with the VL technique and the switched inductor is reported in reference [31]. The converter can achieve significantly high gain, but the converter utilizes two switches operated with different duty ratios, making the control circuitry complex, unlike the proposed converter, which uses a single switch. The VL technique is also presented in [32], where the voltage gain is still less than twice of TBC. Similarly, the converter reported in [33–36] is based on the concept of boosting the input voltage to a very high level; however, the number of components with their voltage and current stress are the main concerns.

An improved voltage lift (iVL) approach is suggested in this literature, combined with a switching inductor network to obtain ultra-high voltage gain. Compared to the conventional voltage lift approach, the improved voltage lift technique needs an additional diode and capacitor, lowering voltage stress on semiconductor devices. In nature, the input current is continuous. Because the proposed topology shares a common connection between the input supply and the load, it is suited for DC Microgrid applications. The technique may be expanded to include *n*-stages.

The following is how the rest of the manuscript is organized: Section 2 examines the suggested topology's derivation, whereas Section 3 describes the proposed converter's operation and steady-state analysis in CCM and DCM. Section 4 analyses the suggested converter in terms of non-idealities, whereas Sections 5 and 6 give parameter suggestions. In Section 7, the *n*-stage converter is discussed. In Section 8, the proposed converter is compared. In Section 9, the hardware findings are provided, and the paper is finally concluded.

2 | TOPOLOGICAL DERIVATION

The switched inductor with the capacitor (SIC), as illustrated in Figure 1a, is a common technique for increasing the boost factor or voltage gain by using this impedance configuration in place of an inductor in a conventional boost converter (TBC). Despite the boost factor being double that of TBC, the switch voltage stress matches the output voltage, much like TBC.

Figure 1b depicts the use of a voltage-lift cell (VL) in an SIC converter (SIC-VL). In comparison to SIC, the SIC-VL converter has one more diode (D_1) and one additional capacitor (C_1). This extra energy storage element raises the SIC's voltage gain by $(1+k)/(1-k)$, where k is the gating signal's duty ratio. When the switch is turned on, the input DC voltage source V_{in} charges this additional capacitor (C_1). In comparison to SIC, C_1 releases more energy to load. The SIC-VL has a voltage gain of $(3-k)/(1-k)$ when using the conventional voltage lift approach, which is an improvement over the SIC converter. In addition, as compared to SIC, the voltage stress on the switch is minimized. The output diode voltage stress is lower than the output voltage.

An improved voltage-lift cell (iVL) is proposed here, as shown in Figure 1c. Compared to conventional voltage-lift cell, the improved cell is refashioned by utilizing an additional diode (D_2) and capacitor (C_2) to improve further and reduce the stress of the SIC. A double stage with an improved VL method converter (dSIC-iVL) is presented in Figure 1d to increase the voltage gain further. In addition, compared to the conventional voltage lift approach, the voltage stress on the output diode is lowered even further, and is equal to half of the output voltage detailed later in the literature.

3 | PROPOSED CONFIGURATION (dSIC-iVL) AND OPERATING PRINCIPLE

Figure 1d shows the suggested configuration of the proposed topology (dSIC-iVL) using iVL cell to obtain the double-stage converter. The configuration consists of a single power switch (S), an SIC impedance network that utilizes two inductors (L_{Z1} and L_{Z2}), two diodes (D_{Z1} and D_{Z2}), and one capacitor (C_Z). The stage 1-improved voltage lift cell in this configuration comprises two diodes (D_1 and D_2) and two energy-storing capacitors (C_1 and C_2). The stage 2-improved voltage lift cell in this configuration comprises two diodes (D_3 and D_4), two energy-storing capacitors (C_3 and C_4), and D_0 is the output diode. The load is taken purely resistive (R). For the proposed converter's steady-state analysis, the inductance of L_{Z1} and L_{Z2} are assumed equal ($L_{Z1} = L_{Z2} = L_Z$). The inductance and capacitance values are sufficiently high so that ripple is negligible. All components are assumed ideal and impedances are linear, time-invariant, and frequency independent. The steady-state analysis is done in continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

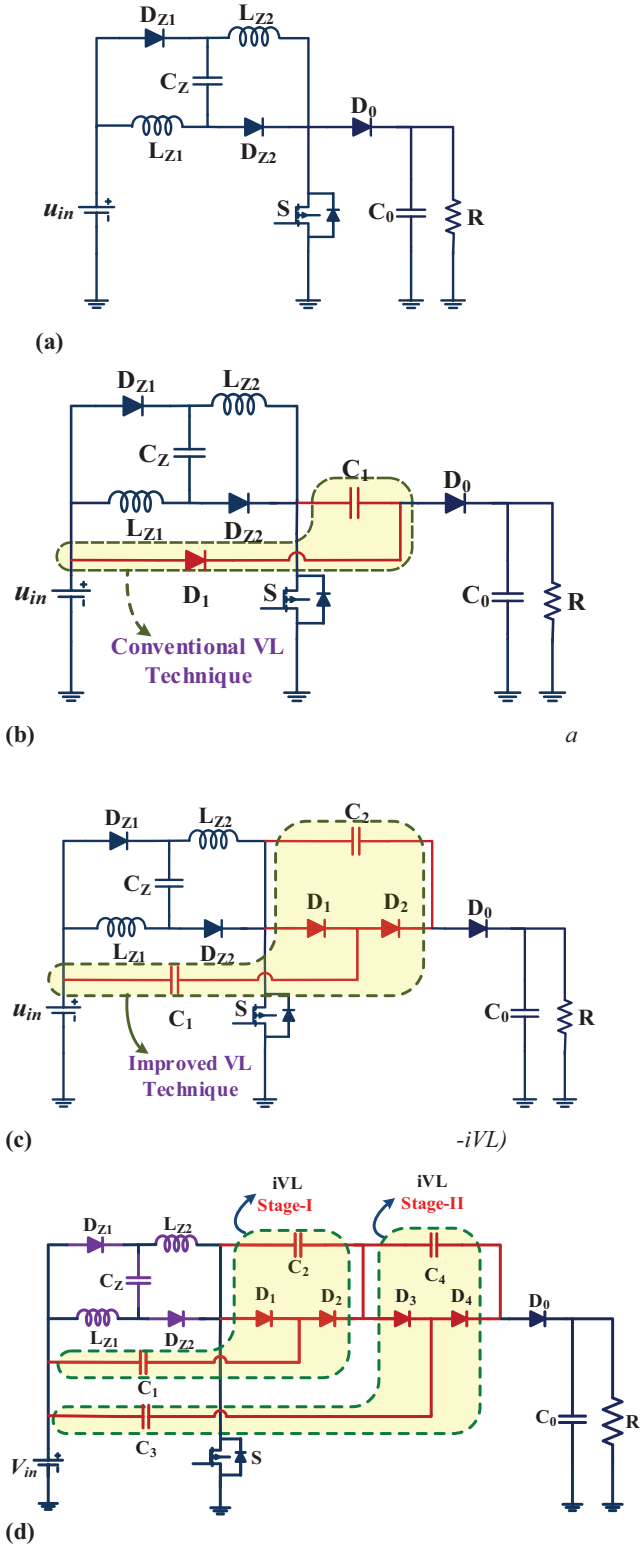

FIGURE 1 (a) Conventional switched inductor boost converter. (b) Application of conventional voltage lift technique to a conventional switched inductor boost converter. (c) Proposed improved voltage technique (SIC-iVL). (d) Proposed configuration for double stage (dSIC-iVL). (a)–(d) Topological derivation of the proposed converter

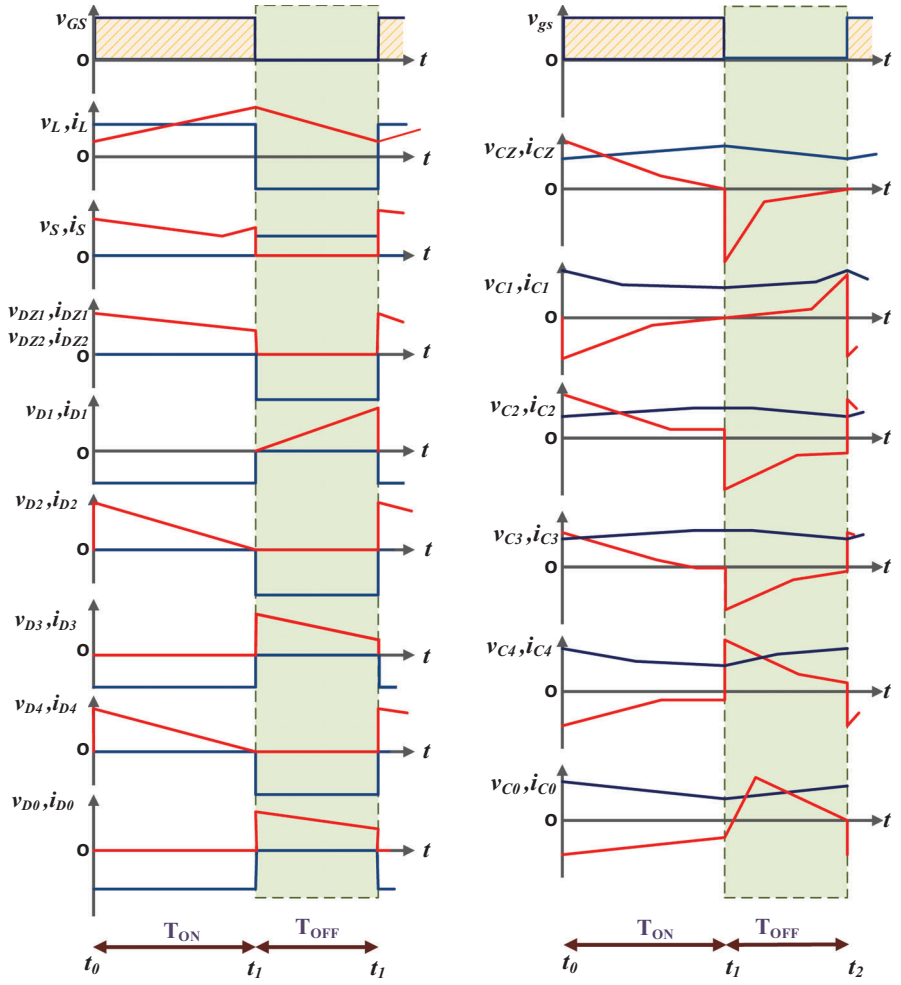

FIGURE 2 Key waveforms in CCM mode

3.1 | CCM operation of the dSIC-iVL converter with equal inductances

When the converter operates in CCM, the converter operates in two modes. The key waveforms are shown in Figure 2. The equivalent topological circuits in both modes are shown in Figure 3a,b.

1. *Mode I:* The power switch is turned *ON*. The equivalent circuit is shown in Figure 3a. V_{in} magnetizes both the inductors L_{Z1} and L_{Z2}. The inductor currents in L_{Z1} and L_{Z2} are equal and rise linearly with equal slope, and reach the maximum value. Diodes D_1, D_3, and D_0 are reversed biased, whereas diodes D_{Z1}, D_{Z2}, D_2, and D_4 are forward biased. The voltage equations of inductors and capacitors in this mode are

$$\begin{cases} v_{LZ1} = v_{LZ2} = v_{CZ} = v_{\text{in}} \\ v_{C2} = v_{\text{in}} + v_{C1} \\ v_{C3} = v_{C1} + v_{C4} \end{cases} \quad (1)$$

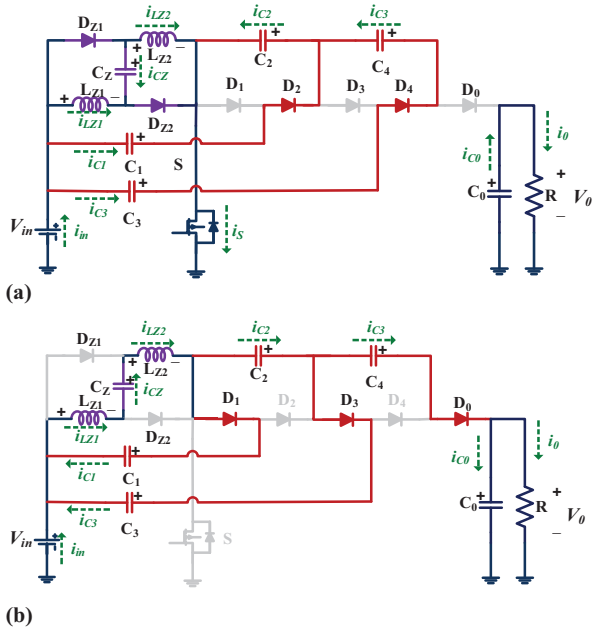

FIGURE 3 (a) Mode I: when the switch is ON. (b) Mode II: when the switch is OFF

2. *Mode II:* The power switch is turned *OFF*. The equivalent circuit is shown in Figure 3b. V_{in} magnetizes both the inductors L_{Z1} and $L_{Z2.}$ The inductor currents in L_{Z1} and L_{Z2} are equal, decrease linearly with an equal slope, and reach the initial value. Diodes D_1, $D_{3,}$ and D_0 are forward biased, whereas diodes D_{Z1}, D_{Z2}, $D_{2,}$ and D_4 are reverse biased. The voltage equations of inductors and capacitors are

$$\begin{cases} v_{LZ1} = v_{LZ2} = \dfrac{v_{CZ} - v_{C1}}{2} = \dfrac{v_{in} - v_{C1}}{2} \\ v_{C3} = v_{C1} + v_{C2} \\ v_O = v_{in} + v_{C3} + v_{C4} \end{cases} \tag{2}$$

Applying inductor voltage second balance on inductor L_{Z1} and L_{Z2} in steady state for the time interval T_S.

$$\begin{cases} \displaystyle\int_0^{T_s} (v_{LZ1} \text{ or } v_{LZ2}).dt = 0 \\ \displaystyle\int_0^{kT_S} v_{in}.dt + \int_{kT_S}^{T_S} \left(\frac{v_{in} - v_{C1}}{2}\right).dt = 0 \\ v_{C1} = \left(\dfrac{1+k}{1-k}\right) v_{in} \end{cases} \tag{3}$$

From (1), (2), and (3), the capacitor voltages can be found as (4)

$$\begin{cases} v_{CZ} = v_{in} \\ v_{C1} = \left(\dfrac{1+k}{1-k}\right) v_{in} \\ v_{C2} = v_{in} + v_{C1} = \dfrac{2v_{in}}{(1-k)} \\ v_{C3} = v_{C1} + v_{C2} = \dfrac{(3+k)\, v_{in}}{(1-k)} \\ v_{C4} = v_{C2} = \dfrac{2v_{in}}{(1-k)} \\ v_{CO} = v_0 = v_{in} + v_{C3} + v_{C4} = \dfrac{6v_{in}}{(1-k)} \end{cases} \tag{4}$$

The relation between the input voltage and output voltage (G_{CCM}) can be found using Equation (4)

$$G_{CCM} = \frac{v_O}{v_{in}} = \frac{6}{(1-k)} \tag{5}$$

The output current (I_o) and input current (I_{in}) relation is given by (7)

$$I_{in} = G_{CCM}\ I_O = \frac{6I_O}{(1-k)} \tag{7}$$

The following relationships of voltage stress of power switch (drain to source v_{DS}) and diodes (cathode to anode) can be derived as

$$\begin{cases} v_{DS} = v_{in} + v_{C1} = \dfrac{2v_{in}}{(1-k)} = \dfrac{v_O}{3} \\ v_{DZ1} = v_{DZ2} = \dfrac{2v_{CZ} - v_{in} + v_{C1}}{2} = \dfrac{v_{in}}{(1-D)} = \dfrac{v_O}{6} \\ v_{D1} = v_{D2} = v_{C2} = \dfrac{2v_{in}}{(1-k)} = \dfrac{v_O}{3} \\ v_{D3} = v_{D4} = v_{C4} = \dfrac{2v_{in}}{(1-k)} = \dfrac{v_O}{3} \\ v_{D0} = v_{in} - v_{in} + v_{C3} = \dfrac{2v_{in}}{(1-k)} = \dfrac{v_O}{3} \end{cases} \tag{8}$$

The average currents through the inductors $L_{Z1} = L_{Z2}$ are $I_{LZ,}$ respectively. The average currents through diode D_{Z1}, D_{Z2}, D_1, D_2, D_3, $D_{4,}$ and D_0 are I_{DZ1}, I_{DZ2}, I_{D1}, I_{D2}, I_{D3}, $I_{D4,}$ and $I_{DO,}$ respectively. And the average current through a single switch is I_S. The average currents can be derived as

$$\begin{cases} I_{LZ1} = I_{LZ2} = I_{LZ} = \dfrac{I_{in}}{2} = \dfrac{3I_O}{(1-k)} \\ I_{DZ1} = I_{DZ2} = \dfrac{I_{in}}{2} = \dfrac{3I_O}{(1-k)} \\ I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D0} = I_O \\ I_S = I_{in} - I_O = \dfrac{(5+k)\, I_O}{(1-k)} \end{cases} \tag{9}$$

3.2 | CCM operation of the dSIC-iVL converter with unequal inductances

The operation of the converter depends on converter parameters. The operation of the converter is somewhat different from the case when inductances of L_{Z1} and L_{Z2} are equal. Two possible situations are considered Case A: $L_{Z1} > L_{Z2}$ and Case B: $L_{Z1} < L_{Z2}$.

3.2.1 | Case A: if inductance L_{Z1} is greater than L_{Z2}

The current waveform through the inductors L_{Z1} and L_{Z2} is shown in Figure 4. The operation of the converter is divided into three modes, as discussed below.

1. *Mode I:* This mode is the same as Mode I, as in the case of equal inductances. The corresponding circuit diagram is the same as Figure 3a. The voltage across the inductors L_{Z1} and L_{Z2} is equal to V_{in}. The inductor currents I_{LZ1} and I_{LZ2} increase linearly with different gradients. The slope of

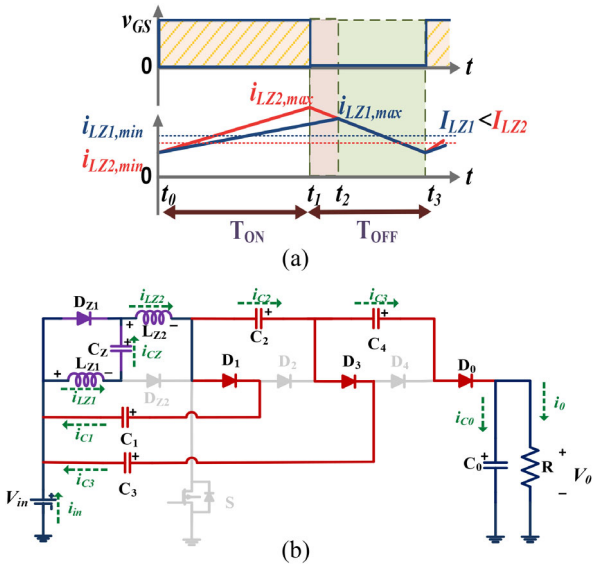

FIGURE 4 (a) Inductor waveforms when $L_{Z1} > L_{Z2}$. (b) Equivalent conduction diagram in Mode II when $L_{Z1} > L_{Z2}$

inductor currents of L_{Z1} and L_{Z2} can be achieved as

$$\begin{cases} \dfrac{di_{LZ1}}{dt} = \dfrac{v_{\text{in}}}{L_{Z1}} \\ \dfrac{di_{LZ2}}{dt} = \dfrac{v_{\text{in}}}{L_{Z2}} \end{cases} \tag{10}$$

2. *Mode II:* At the start of this mode, the switch is turned OFF. This mode occurs for a short duration of λT_S, as shown in Figure 4b. The corresponding circuit diagram is shown in Figure 4b. Diodes D_{Z1}, D_1, D_3, and D_0 are forward biased, while diodes D_{Z2}, D_2, and D_4 are reverse biased. Inductor current I_{LZ1} is smaller than I_{LZ2}, as shown in Figure 4a. The inductor L_1 charges during this period with a constant positive gradient, and the current L_{Z2} has a large negative slope and discharge during this mode. The slope of inductor currents of L_{Z1} and L_{Z2} can be achieved as

$$\begin{cases} \dfrac{di_{LZ1}}{dt} = \dfrac{v_{CZ}}{L_{Z1}} = \dfrac{v_{\text{in}}}{L_{Z1}} \\ \dfrac{di_{LZ2}}{dt} = \dfrac{-v_{C1}}{L_{Z2}} \end{cases} \tag{11}$$

3. *Mode III:* This mode is the same as Mode II, as in the case of equal inductances. The corresponding circuit diagram is shown in Figure 3b. It can be seen that inductors L_{Z1} and L_{Z2} are in series. Diodes D_1, D_3, and D_0 are forward biased, while diodes D_{Z1}, D_{Z2}, D_2, and D_4 are reverse biased. The currents in the inductors L_{Z1} and L_{Z2} demagnetize with an equal negative slope which can be achieved as follows:

$$\begin{cases} \dfrac{di_{LZ1}}{dt} = \dfrac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}} \\ \dfrac{di_{LZ2}}{dt} = \dfrac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}} \end{cases} \tag{12}$$

According to voltage second principle balance, the average voltage across the inductor is null. Therefore,

$$\begin{cases} \displaystyle\int_0^{T_s} v_{LZ1}\,.dt = 0 \\ \displaystyle\int_0^{(k+\lambda)T_S} v_{\text{in}}.dt + \int_{(k+\lambda)T_S}^{T_S} L_{Z1}\left(\frac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}}\right).\,dt = 0 \end{cases} \tag{13}$$

$$\begin{cases} \displaystyle\int_0^{T_s} v_{LZ2}\,.dt = 0 \\ \displaystyle\int_0^{(k+\lambda)T_S} v_{\text{in}}.dt + \int_{kT_S}^{T_S} L_{Z2}\left(\frac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}}\right).\,dt = 0 \end{cases} \tag{14}$$

On solving (13) and (14) and using voltage relations (1) and (2), it is found that that voltage gain is unaffected as given by relation by Equation (5) i.e.

$$\frac{v_0}{v_{\text{in}}}|_{LZ1>LZ2} = \frac{6}{(1-k)} \tag{15}$$

From Figure 4a it is clear that the average value of the inductor currents is not equal. It can be noted that the average value of inductor current I_{LZ2} is greater than I_{LZ1}.

3.2.2 | Case B: if inductance L_{Z2} is greater than L_{Z1}

Similar to Case A, the operation of the converter is divided into three modes, as discussed below. The current waveform through the inductors L_{Z1} and L_{Z2} is shown in Figure 5. The three modes of operation are discussed in this section.

1. *Mode I:* This mode is the same as Mode I, as in the case of equal inductances. The corresponding circuit diagram is the same as Figure 3a. The voltage across the inductors L_{Z1} and L_{Z2} is equal to V_{in}. The inductor currents I_{LZ1} and I_{LZ2} increase linearly with different gradients. The slope of inductor currents of L_{Z1} and L_{Z2} can be achieved as

$$\begin{cases} \dfrac{di_{LZ1}}{dt} = \dfrac{v_{\text{in}}}{L_{Z1}} \\ \dfrac{di_{LZ2}}{dt} = \dfrac{v_{\text{in}}}{L_{Z2}} \end{cases} \tag{16}$$

2. *Mode II:* At the start of this mode, the switch is turned OFF. This mode occurs for a short duration of λT_S, as shown in Figure 5b. The corresponding circuit diagram is shown in Figure 5b. Diodes D_{Z2}, D_1, D_3, and D_0 are forward biased, while diodes D_{Z1}, D_2, and D_4 are reverse biased. Inductor current I_{LZ2} is smaller than I_{LZ1}, as shown in Figure 5a. The inductor L_{Z2} charges during this period with a constant positive gradient, and the current L_{Z1} has a large negative slope and discharge in this period. The

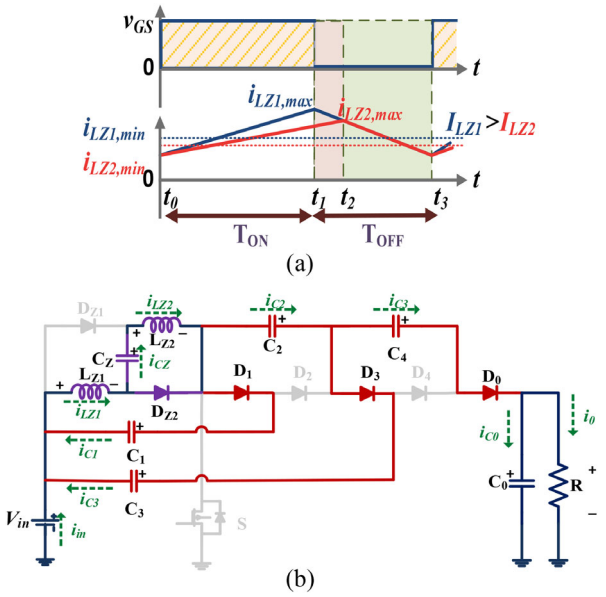

FIGURE 5 (a) Inductor waveforms when $L_{Z2} > L_{Z1}$. (b) Equivalent conduction diagram in Mode II when $L_{Z2} > L_{Z1}$

slope of inductor currents of L_{Z1} and L_{Z2} can be achieved as

$$\begin{cases} \dfrac{di_{LZ1}}{dt} = \dfrac{-v_{C1}}{L_{Z1}} \\ \dfrac{di_{LZ2}}{dt} = \dfrac{v_{CZ1}}{L_{Z2}} \end{cases} \tag{17}$$

3. *Mode III:* This mode is the same as Mode II, as in the case of equal inductances. The corresponding circuit diagram is shown in Figure 3b. It can be seen that inductors L_{Z1} and L_{Z2} are in series. Diodes D_1, D_3, and D_0 are forward biased, while diodes D_{Z1}, D_{Z2}, D_2, and D_4 are reverse biased. The current in the inductors L_{Z1} and L_{Z2} demagnetize with an equal negative slope which can be achieved as follows:

$$\begin{cases} \dfrac{di_{LZ1}}{dt} = \dfrac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}} \\ \dfrac{di_{LZ2}}{dt} = \dfrac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}} \end{cases} \tag{18}$$

According to voltage second principle balance, the average of voltage across the inductor is null. Therefore,

$$\begin{cases} \displaystyle\int_0^{T_s} v_{LZ1}\,.dt = 0 \\ \displaystyle\int_0^{(k+\lambda)T_S} v_{\text{in}}.dt + \int_{kT_S}^{T_S} L_{Z1}\left(\frac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}}\right).\,dt = 0 \end{cases} \tag{19}$$

$$\begin{cases} \displaystyle\int_0^{T_s} v_{LZ2}\,.dt = 0 \\ \displaystyle\int_0^{(k+\lambda)T_S} v_{\text{in}}.dt + \int_{(k+\lambda)T_S}^{T_S} L_{Z2}\left(\frac{v_{\text{in}} - v_{C1}}{L_{Z1} + L_{Z2}}\right).\,dt = 0 \end{cases} \tag{20}$$

On solving (19) and (20) and using voltage relations (1) and (2), it is found that that voltage gain is unaffected as given by relation by Equation (5) i.e.

$$\frac{v_0}{v_{\text{in}}}|_{LZ2>LZ1} = \frac{6}{(1-k)} \tag{21}$$

From Figure 5a, it is clear that the average value of the inductor currents is not equal. It can be noted that the average value of inductor current I_{LZ1} is greater than I_{LZ2}.

3.3 | DCM operation of the dSIC-iVL converter

The proposed dSIC-iVL converter works in DCM mode the instant inductor currents to zero. There are three different working modes: Mode I, Mode II, and Mode III. The key waveforms are shown in Figure 6a.

1. *Mode I:* In this mode, the working principle of the converter is the same as Mode I of the CCM operation. The maximum or peak value of the inductor currents through L_{Z1} and L_{Z2} can be calculated using Equation (22).

$$i_{LZ1,\,\text{peak}} = i_{LZ2,\,\text{peak}} = \frac{v_{\text{in}} k T_S}{L_Z} \tag{22}$$

2. *Mode II:* Power switch S is *OFF* in this mode. The inductors are demagnetized from peak value to zero at the end of the $k_1 T_S$ period. The maximum or peak value of the inductor currents through L_{Z1} and L_{Z2} can be calculated using Equation (23).

$$i_{LZ1,\,\text{peak}} = i_{LZ2,\,\text{peak}} = \frac{(v_{C1} - v_{\text{in}})\, k_1 T_S}{2L_Z} \tag{23}$$

3. *Mode III:* The power switch is still OFF in this mode. The energy stored in both the inductor is zero because the current in the inductors is zero. Therefore, the voltage across the inductors is zero. The equivalent circuit is shown in Figure 6b. The energy stored in capacitors C_0 is supplied to the load.

Equating ripple values from (22) and (23), the capacitor voltage C_1 can be found as

$$v_{C1} = \left(\frac{2k + k_1}{k_1}\right) v_{\text{in}} \tag{26}$$

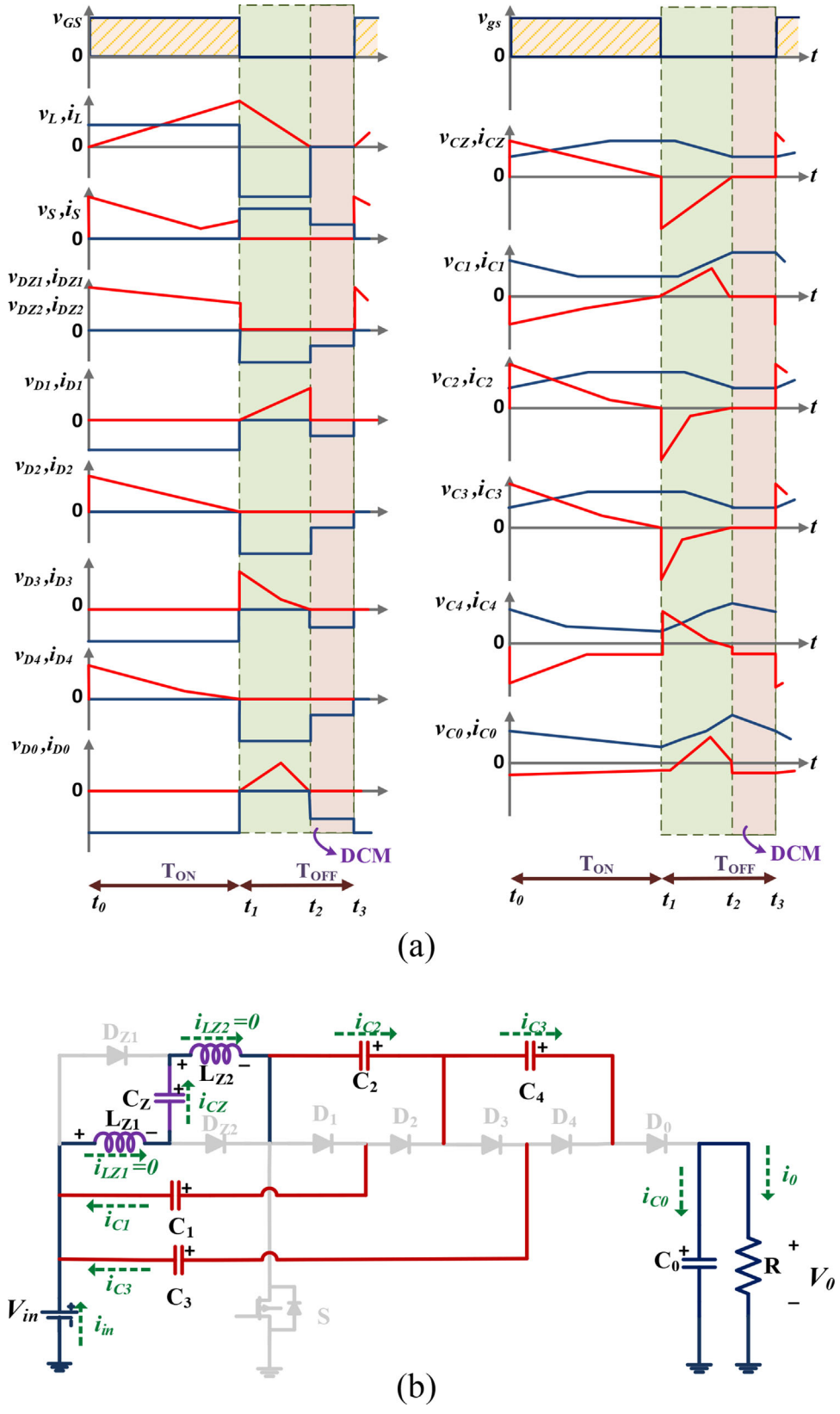

FIGURE 6 (a) Key waveforms in DCM mode. (b) Mode III: DCM

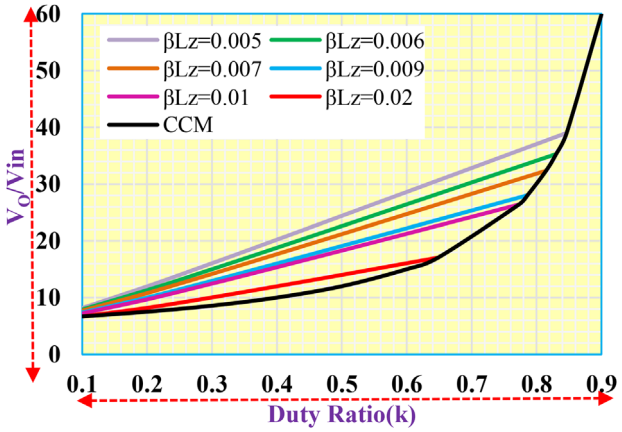

FIGURE 7 Voltage gain in DCM mode

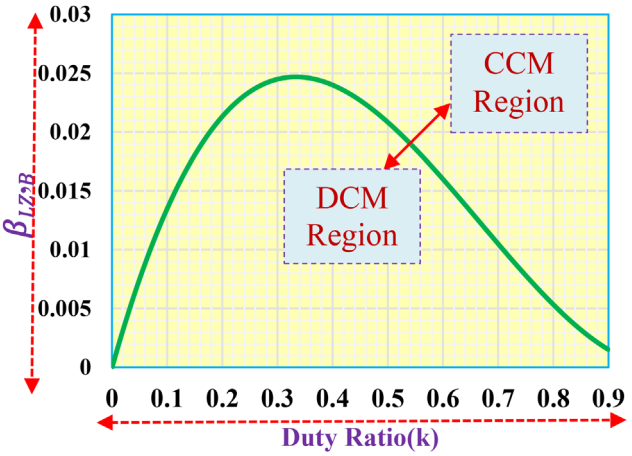

FIGURE 8 Unified inductor time constant ($\beta_{LZ,B}$) versus duty ratio (k)

$$\begin{cases} v_{C2} = v_{\text{in}} + v_{C1} = \dfrac{2(k+k_1)v_{\text{in}}}{k_1} \\ v_{C3} = v_{C1} + v_{C2} = \dfrac{(4k+3k_1)v_{\text{in}}}{k_1} \\ v_{C4} = v_{C2} = \dfrac{2(k+k_1)v_{\text{in}}}{k_1} \\ v_O = v_{\text{in}} + v_{C3} + v_{C4} = \dfrac{6(k+k_1)v_{\text{in}}}{k_1} \end{cases} \tag{27}$$

Also, it can be noted from waveforms from Figure 6 that, in Mode II and using geometry

$$\frac{1}{2}\left(\frac{v_{\text{in}} k T_S}{L_Z}\right) k_1 = I_{D0} + I_{D1} + I_{D3} = 3I_O \tag{28}$$

From (27) and (28), the following quadratic can be obtained as

$$\left(\frac{v_O}{v_{\text{in}}}\right)^2 - 6\left(\frac{v_O}{v_{\text{in}}}\right) - \frac{6k^2}{\beta_{LZ}} = 0 \tag{29}$$

where $\beta_{LZ} = \frac{6L_Z}{RT_S}$ is the unified inductor time constant.

The second voltage gain (G_{DCM}) of the *dSIC-iVL* converter can be found using relation from (30) (Figure 7)

$$G_{DCM} = \left(\frac{v_O}{v_{\text{in}}}\right) = 3\left(1 + \sqrt{1 + \frac{2k^2}{3\beta_{Lz}}}\right) \tag{30}$$

3.4 | Boundary mode operation of the dSIC-iVL converter

It is assumed that the proposed converter dSIC-iVL is operated at the boundary of CCM and DCM. The voltage gains of both CCM and DCM are equal. Therefore

$$G_{CCM} = G_{DCM} \tag{31}$$

The boundary unified inductor normalized time $\beta_{LZ,B}$ the constant can be derived as

$$\beta_{LZ,B} = \frac{k(1-k)^2}{6} \tag{32}$$

The unified inductor time constant versus duty ratio is depicted in Figure 8. If $\beta_{LZ} > \beta_{LZ,B}$ then converter operated in CCM mode and if $\beta_{LZ} < \beta_{LZ,B}$ the converter operated in DCM mode. The maximum value of $\beta_{LZ,B}$ occurs at $k = 0.33$ and is equal to 0.02169.

4 | PRACTICAL MODEL OF THE dSIC-iVL CONVERTER

In actuality, the converter will have non-idealities that were not considered in the previous analysis. The losses that occur in each component may impact the converter's efficiency. This section calculates the influence of various non-idealities on efficiency and non-ideal voltage gain expression. The inductors' dc resistance is r_L, the capacitance's equivalent series resistance is r_C, the power switch's *ON* resistance is r_S, the forward voltage drop of the diodes is v_D, and the on resistance is r_D. Figure 9 depicts the analogous non-ideal model.

4.1 | Power loss in the switch S

The conduction loss of the power switch (S) is mainly due to the ON resistance of the switch, and root means square (RMS) current through the switch. The current through the switch can be expressed by

$$i_S = \begin{cases} i_{\text{in}} - i_O & 0 < t < kT_S \\ 0 & kT_S < t < T_S \end{cases} \tag{33}$$

The conduction loss ($P_{S,\text{conduction}}$) in the switch can be calculated using Equation (33) as

$$P_{S,\text{conduction}} = {i_{S_{rms}}}^2 . r_S = \frac{1}{k}\left(\frac{1+k}{(1-k)} I_O\right)^2 r_S \tag{34}$$

$$P_{S,\text{conduction}} = \frac{(5+k)^2}{k(1-k)^2}\frac{r_S}{R} P_O \tag{35}$$

where $P_o = {I_o}^2 R = 200$ W is the output power of the load.

The total switching loss ($P_{S,\text{switching}}$) of the power switch (S) can be expressed as

$$P_{S,\text{switching}} = \begin{cases} \frac{1}{T_S}\left(t_r + t_f\right) . I_S v_S \\ \frac{1}{T_S}\left(t_r + t_f\right)\frac{(5+k)}{3(1-k)} P_o \end{cases} \tag{36}$$

where t_r and t_f are rising and falling times of the MOSFET during turning *ON* and *OFF*.

The total loss ($P_{S,\text{total}}$) in the switch is the sum of conduction and switching loss.

$$P_{S,\text{total}} = \frac{(5+k)^2}{k(1-k)^2}\frac{r_S}{R} P_O + \frac{1}{T_S}\left(t_r + t_f\right)\frac{(5+k)}{3\,(1-k)} P_o \tag{37}$$

Let $r_S =$ 10 mΩ, and $(t_r + t_f) =$ 34.71 ns, the total loss in the switches is equal to 3.33 W.

4.2 | Power loss in the inductors L_{Z1} and L_{Z2}

The total conduction loss ($P_{L,\text{total}}$) due to dc resistance of inductor can be obtained as

$$P_{L,\text{total}} = \begin{cases} ({I_{LZ1}}_{rms}^2 + {I_{LZ1}}_{rms}^2) r_L = 2\left(\frac{3I_o}{1-k}\right)^2 r_L \\ \frac{18}{(1-k)^2}\frac{r_L}{R} P_O \end{cases} \tag{38}$$

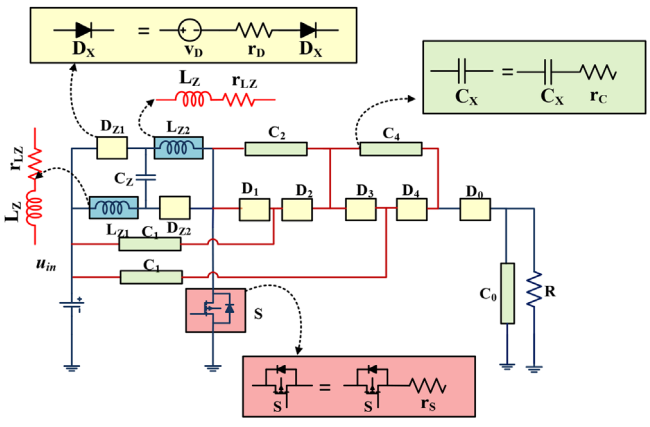

FIGURE 9 A practical model of the dSIC-iVL converter

Let dc resistance of the inductor be equal to 0.1 Ω. The total ohmic loss equals 5.62 W.

4.3 | Power loss in the diodes D_{Z1}, D_{Z2}, and D_0 to D_4

The losses in the diodes depend on current flow and forward voltage drop. The total losses in all diodes are given as

$$P_{D,\text{total}} = \sum_{j=0}^{4}\left(v_{Dj} I_{Dj} + {I_{Dj}}_{rms}^2 r_{Dj}\right) \times \sum_{j=1}^{2}\left(v_{DZj} I_{DZj} + {I_{DZj}}_{rms}^2 r_{DZj}\right) \tag{39}$$

$$P_{DZ1} = P_{DZ2} = \begin{cases} v_D\left(\frac{3I_O}{1-k}\right) + \frac{(3I_O)^2}{k(1-k)^2} r_D \\ \frac{3}{(1-k)}\frac{v_D}{v_O} P_O + \frac{9}{k(1-k)^2}\frac{r_D}{R} P_O \end{cases} \tag{40}$$

$$P_{D1} = P_{D3} = \begin{cases} v_D I_O + \frac{{I_O}^2}{(1-k)} r_D \\ \frac{v_D}{v_O} P_O + \frac{1}{(1-k)}\frac{r_D}{R} P_O \end{cases} \tag{41}$$

$$P_{D2} = P_{D4} = \begin{cases} v_D I_O + \frac{{I_O}^2}{k} r_D \\ \frac{v_D}{v_O} P_O + \frac{1}{k}\frac{r_D}{R} P_O \end{cases} \tag{42}$$

The total power loss ($P_{D,\text{total}}$) is the summation of all the power losses occurring in diodes.

$$P_{D,\text{total}} = \begin{cases} P_{DZ1} + P_{DZ2} + P_{DO} + P_{D1} + P_{D2} + P_{D3} + P_{D4} \\ \frac{2\,(5-k)}{(1-k)}\frac{v_D}{v_O} P_O + \frac{2\,(10-k)}{k(1-k)^2}\frac{r_D}{R} P_O \end{cases} \tag{43}$$

Let $v_D =$ 0.4 V and $r_D =$ 10 mΩ, the total loss occurring in diodes can be calculated as 7.34 W.

4.4 | Power loss in the capacitors C_Z and C_1 to C_4

The losses occurring in the capacitors depend on the current through the capacitors. The power losses ($P_{C,\text{total}}$) of the capacitors due to their equivalent series resistance (ESR) (r_{CX}) can be

obtained as follows:

$$P_{C,\text{total}} = \sum_{j=1}^{4} \left({I_{Cj_{rms}}}^2 r_C \right) + {I_{CZ_{rms}}}^2 r_C \tag{44}$$

The mean square value of current through capacitors can be found using the following formula (45)

$${I_{C_{\text{rms}}}}^2 = \frac{\int_0^{DT_S} i_{C_{\text{on}}} + \int_{DT_S}^{T_S} i_{C_{\text{off}}}}{T_S} \tag{45}$$

The mean square values (${I_{C\varkappa_{rms}}}^2$) of current through capacitors are expressed in Equation (46)

$$\begin{cases} {I_{CZ_{rms}}}^2 = \dfrac{9{I_O}^2}{k\,(1-k)} \\ {I_{C1_{rms}}}^2 = \dfrac{{I_O}^2}{k\,(1-k)} \\ {I_{C2_{rms}}}^2 = \dfrac{4{I_O}^2}{k\,(1-k)} \\ {I_{C3_{rms}}}^2 = \dfrac{{I_O}^2}{k\,(1-k)} \\ {I_{C4_{rms}}}^2 = \dfrac{{I_O}^2}{k\,(1-k)} \end{cases} \tag{46}$$

The total power loss in capacitors ($P_{C,\text{total}}$) can be calculated as

$$P_{C,\text{total}} = \begin{cases} \left({I_{C1_{rms}}}^2 + {I_{C2_{rms}}}^2 + {I_{C3_{rms}}}^2 + {I_{C4_{rms}}}^2 + {I_{C02_{rms}}}^2 \right) r_C \\ \dfrac{16}{k\,(1-k)} \dfrac{r_C}{R} P_O \end{cases} \tag{47}$$

Let ESR of capacitors be equal to 66 mΩ. The total ohmic loss equals 2.2 W.

4.5 | Efficiency calculation

The efficiency (η) of the *dSIC-iVL* converter can be expressed as

$$\eta = \frac{P_o}{P_o + P_{\text{total,loss}}} \tag{48}$$

$P_{\text{total,loss}}$ is the total loss occurring in the proposed converter and equal to the sum of losses occurring in the switch, inductors, diodes, and capacitors i.e.

$$P_{\text{total,loss}} = P_{S,\text{ total}} + P_{L,\text{total}} + P_{D,\text{total}} + P_{C,\text{total}} \tag{49}$$

$$= \left(A_1 \frac{r_S}{R} + A_2 \frac{r_L}{R} + A_3 \frac{r_D}{R} + A_4 \frac{r_C}{R} + A_5 \frac{v_D}{v_O} + A_6 \right) \times P_o = 16.68\ \text{W}$$

where

$$\begin{cases} A_1 = \dfrac{(5+k)^2}{k(1-k)^2}\,,\ A_2 = \dfrac{18}{(1-k)^2}\,,\ A_3 = \dfrac{2\,(10-k)}{k(1-k)^2} \\ A_4 = \dfrac{16}{k\,(1-k)}\,,\ A_5 = \dfrac{2\,(5-k)}{(1-k)}\,,\ A_6 = \dfrac{\left(t_r + t_f\right)}{3T_S} \dfrac{(5+k)}{(1-k)} \end{cases}$$

Therefore, the efficiency can be expressed and calculated as

$$\eta\% = \frac{1}{1 + A_1 \frac{r_S}{R} + A_2 \frac{r_L}{R} + A_3 \frac{r_D}{R} + A_4 \frac{r_C}{R} + A_5 \frac{v_D}{v_O} + A_6} \times 100\% = 92.3\% \tag{50}$$

4.6 | Practical voltage gain

The ideal voltage gain of the proposed converter is derived in (5) as

$$G_{CCM} = \frac{v_O}{v_{\text{in}}} = \frac{6}{(1-k)} \tag{51}$$

Thus, the practical voltage gain can be expressed as in Equation (52).

$$G_{CCM_{practical}} = \frac{v_0}{v_{\text{in}}}\,\eta = \frac{6}{(1-\text{k})} \times \frac{1}{\left(1 + A_1 \frac{r_S}{R} + A_2 \frac{r_L}{R} + A_3 \frac{r_D}{R} + A_4 \frac{r_C}{R} + A_5 \frac{v_D}{V_o} + A_6 \right)} \tag{52}$$

5 | PARAMETER DESIGN OF PASSIVE COMPONENTS

The selection of components depends upon the duty cycle (k), switching frequency (f_S), and load resistance (R)

5.1 | Selection of inductors

The ripple in the inductor currents L_{Z1} and L_{Z2} can be obtained during the state when the switch is *ON*.

$$\begin{cases} \Delta\, i_{LZ1} = \dfrac{v_{CZ} k}{L_{Z1} f_S} = \dfrac{k v_{\text{in}}}{L_{Z1} f_S} \\ \Delta\, i_{LZ2} = \dfrac{v_{CZ} k}{L_{Z2} f_S} = \dfrac{k v_{\text{in}}}{L_{Z2} f_S} \end{cases} \tag{53}$$

Hence the inductance value of L_{Z1} and L_{Z2} is calculated using equations

$$\begin{cases} L_{Z1} = \dfrac{v_{\text{in}}k}{\Delta i_{LZ1} f_S} = \dfrac{v_{\text{in}}k}{r_{LZ1}\%I_{LZ1} f_S} \\ L_{Z2} = \dfrac{v_{\text{in}}k}{\Delta i_{LZ2} f_S} = \dfrac{v_{\text{in}}k}{r_{LZ1}\%I_{LZ2} f_S} \end{cases} \tag{54}$$

where $r_{L1}\%$ and $r_{L2}\%$ is percentage ripple allowed in the inductor currents L_{Z1} and L_{Z2}. By considering peak to peak ripple of 1.5 A, the value of inductances can be calculated as

$$L_{Z1} = L_{Z2} = \frac{v_{\text{in}}k}{\Delta i_{LZ1} f_S} = \frac{20 \times 0.6}{1.5\text{A} \times 50\ \text{kHz}} = 0.16\ \text{mH}$$

So the value of L_{Z1} and L_{Z2} can be selected as greater than 0.16 mH.

The following equation in (55) and (56) must be valid to operate the inductors in *CCM* mode.

$$\begin{cases} I_{LZ1} - \dfrac{\Delta i_{LZ1}}{2} > 0 \\ I_{LZ2} - \dfrac{\Delta i_{LZ2}}{2} > 0 \end{cases} \tag{55}$$

$$\begin{cases} L_{Z1} > \dfrac{k(1-k)^2 R}{36 f_S} \\ L_{Z2} > \dfrac{k(1-k)^2 R}{36 f_S} \end{cases} \tag{56}$$

5.2 | Selection of capacitors

The value of capacitors depends on the voltage ripple, duty ratio (k), switching frequency (f_S), and load resistance (R). The capacitors C_Z, C_0 to C_4 can be selected by considering peak to peak ripple as 4 V.

$$\begin{cases} \Delta v_{CZ} = \dfrac{|Q_{CZ}|}{C_Z} = \dfrac{3v_o}{R f_S C_Z} \\ C_Z \geq \dfrac{3v_o}{R f_S r_{CZ}\% v_{CZ}} \\ C_Z \geq \dfrac{3 \times 300}{400 \times 50\ \text{kHz} \times 4\ \text{A}} = 11.25\ \mu F \end{cases} \tag{57}$$

$$\begin{cases} \Delta v_{C1} = \dfrac{|Q_{C1}|}{C_1} = \dfrac{v_o}{R f_S C_1} \\ C_1 \geq \dfrac{v_o}{R f_S r_{C1}\% v_{C1}} \\ C_1 \geq \dfrac{300}{400 \times 50\ \text{kHz} \times 4A} = 3.75\ \mu F \end{cases} \tag{58}$$

$$\begin{cases} \Delta v_{C2} = \dfrac{|Q_{C2}|}{C_2} = \dfrac{2v_o}{R f_S C_2} \\ C_2 \geq \dfrac{2v_o}{R f_S r_{C2}\% v_{C2}} \\ C_2 \geq \dfrac{2 \times 300}{400 \times 50\ \text{kHz} \times 4A} = 7.5\ \mu F \end{cases} \tag{59}$$

$$\begin{cases} \Delta v_{C3} = \dfrac{|Q_{C3}|}{C_3} = \dfrac{v_o}{R f_S C_3} \\ C_3 \geq \dfrac{v_o}{R f_S r_{C3}\% v_{C3}} \\ C_3 \geq \dfrac{300}{400 \times 50\ \text{kHz} \times 4A} = 3.75\ \mu F \end{cases} \tag{60}$$

$$\begin{cases} \Delta v_{C4} = \dfrac{|Q_{C4}|}{C_4} = \dfrac{v_o}{R f_S C_4} \\ C_4 \geq \dfrac{v_o}{R f_S r_{C4}\% v_{C4}} \\ C_4 \geq \dfrac{300}{400 \times 50\text{kHz} \times 4A} = 3.75\mu\ F \end{cases} \tag{61}$$

$$\begin{cases} \Delta v_{C0} = \dfrac{|Q_{C0}|}{C_o} = \dfrac{v_o k}{R f_S C_0} \\ C_0 \geq \dfrac{v_o k}{R f_S r_{C0}\% v_o} \\ C_0 \geq \dfrac{0.6 \times 300}{400 \times 50\text{kHz} \times 4A} = 2.25\ \mu F \end{cases} \tag{62}$$

where $r_{CZ}\%$, $r_{C1}\%$, $r_{C2}\%$, $r_{C3}\%$, $r_{C4}\%$, and $r_{C0}\%$ is percentage ripple allowed in capacitor voltages. The suitable capacitance value can be selected using Equations (57) to (62). The output capacitor C_0 is selected as 220 μF/450 V, while the rest capacitors are selected as 220 μF/250V.

6 | PARAMETER DESIGN OF SEMICONDUCTOR DEVICES

Power switch and diode parameter selection is based on their current and voltage stresses, reported in Table 1 and estimated in Section 3.

For the prototype of rating 20 V/300 V, voltage rating must be greater than 100 V and current ratings greater than the input current. C3M0065090J Silicon Carbide Power MOSFET is selected with blocking voltage of 900 V and STTH30R04, ultra-fast recovery diodes are selected with blocking voltage up to 900 V.

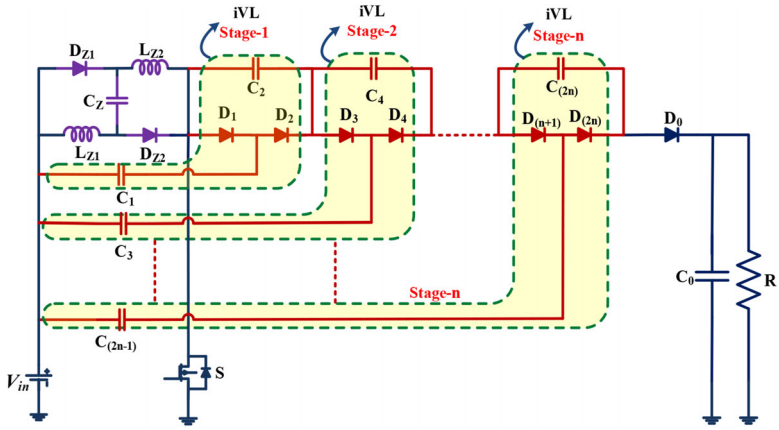

FIGURE 10 Proposed *n*-stage converter (nSIC-iVL)

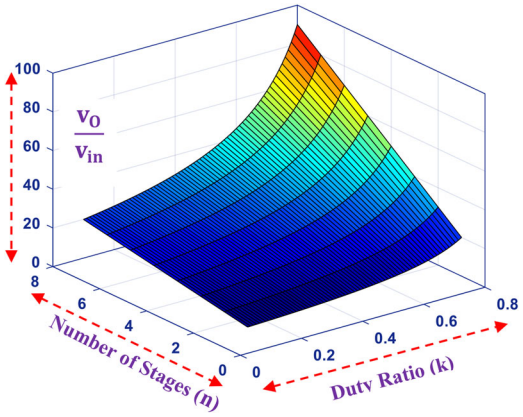

FIGURE 11 Ideal voltage gain of *n*-stage converter (nSIC-iVL)

7 | PROPOSED *n*-STAGE CONVERTER (nSIC-iVL) CONVERTER

The double-stage converter dSIC-iVL can be extended into *n*-stages. The nSIC-iVL converter has a single switch *S* two inductors, L_{Z1} and L_{Z2}. The converter has a single input source V_{in} and a single load. The total number of capacitors in the *n*-stage structure equals (2*n*+2) and the total number of diodes is (2*n*+3). The circuit diagram is shown in Figure 10

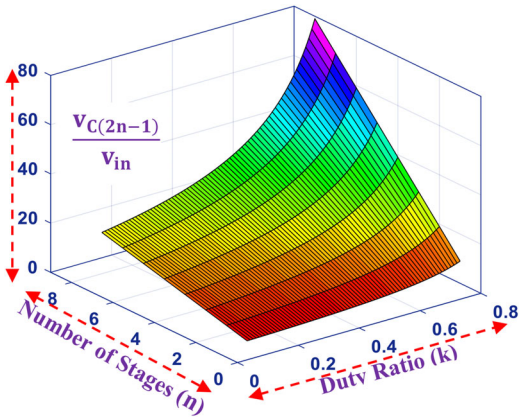

FIGURE 12 Odd capacitor voltages of *n*-stage converter (nSIC-iVL)

Based on the analysis in Section 3, the voltage gain ($G_{\text{n-CCM}}$) in CCM of the *n*-stage proposed nSIC-iVL converter can be expressed as

$$G_{n-CCM} = \frac{v_{\text{O}}}{v_{\text{in}}} = \frac{2\,(n+1)}{(1-k)} \tag{63}$$

The voltage gain (G_{n-CCM}) of the *n*-stage proposed converter is depicted in Figure 11 for different stages and duty ratios.

The capacitor voltages of the *n*-stage proposed *nSIC-iVL* converter can be expressed as

$$\begin{cases} v_{CZ} = v_{\text{in}} \\ v_{C1} = \dfrac{1+k}{1-k}\, v_{\text{in}} \\ v_{C2} = \dfrac{2}{(1-k)}\, v_{\text{in}} \\ v_{C3} = \dfrac{(3+k)}{(1-k)}\, v_{\text{in}} \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ v_{C(2n-1)} = \dfrac{(2n-1+k)}{(1-k)}\, v_{\text{in}} \\ v_{C(2n)} = \dfrac{2}{(1-k)}\, v_{\text{in}} \\ v_{CO} = \dfrac{2\,(n+1)}{(1-\text{k})}\, v_{\text{in}} \end{cases} \tag{64}$$

The capacitor voltage of the *n*-stage proposed converter (nSIC-iVL) is depicted in Figures 12 and 13 for different stages and duty ratios.

TABLE 1 Voltage and current stress of semiconductors

Semiconductor	Voltage stress	Current stress
Switch S	$v_O/3$	$(5+k)I_o/(1-k)$
Diode D_{Z1}	$v_O/6$	$3I_o/(1-k)$
Diode D_{Z2}	$v_O/6$	$3I_o/(1-k)$
Diode D_1	$v_O/3$	I_o
Diode D_2	$v_O/3$	I_o
Diode D_3	$v_O/3$	I_o
Diode D_4	$v_O/3$	I_o
Output diode Do	$v_O/3$	I_o

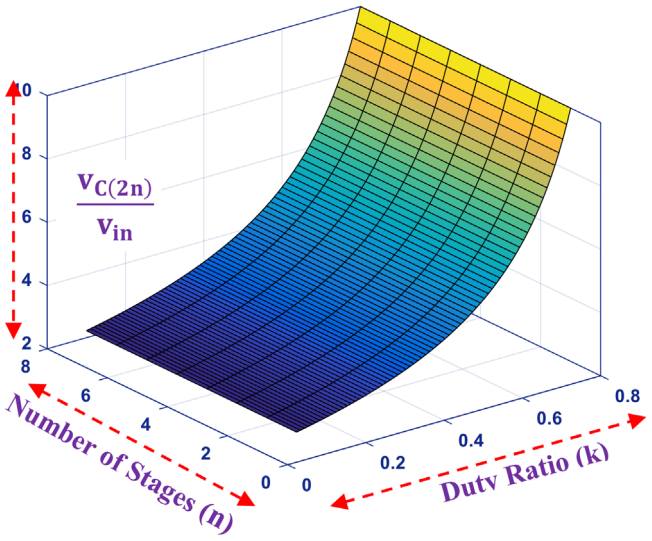

FIGURE 13 Even capacitor voltages of n-stage converter (nSIC-iVL)

The voltage stress on the switch (drain to source v_{DS}) and diodes (cathode to anode) can be expressed as

$$\begin{cases} v_{DS} = \dfrac{v_O}{(n+1)} \\ v_{DZ1} = v_{DZ2} = \dfrac{v_O}{2(n+1)} \\ v_{D1} = \dfrac{v_O}{(n+1)} \\ \vdots \\ v_{D(2n-1)} = v_{D(2n)} = \dfrac{v_O}{(n+1)} \\ v_{D0} = \dfrac{v_O}{(n+1)} \end{cases} \tag{65}$$

The normalized stress on semiconductors (diodes and switches) is shown in Figure 14. The voltage stress on the semiconductor devices reduces as the number of stages increases.

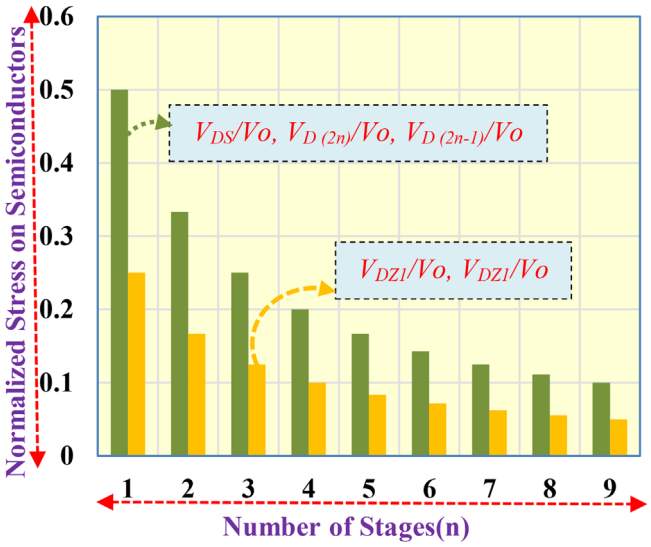

FIGURE 14 Normalized voltage stress on semiconductor of n-stage converter (nSIC-iVL)

The average input current (I_{in}) can be expressed as

$$I_{in} = \frac{2(n+1)}{(1-k)} I_O \tag{66}$$

The average inductor currents of inductors L_{Z1} and L_{Z2} can be expressed as

$$I_{LZ1} = I_{LZ2} = I_{LZ} = \frac{I_{in}}{2} = \frac{(n+1)}{(1-k)} I_O \tag{67}$$

The average currents through diodes can be expressed as

$$\begin{cases} I_{DZ1} = I_{DZ2} = \dfrac{I_{in}}{2} = \dfrac{(n+1)}{(1-k)} I_O \\ I_{D(2n-1)} = I_{D(2n)} = I_{D0} = I_O \end{cases} \tag{68}$$

The average current through switch (S) can be expressed as

$$I_S = I_{in} - I_O = \frac{(2n+k+1)}{(1-k)} I_O \tag{69}$$

8 | COMPARISON WITH THE SIMILAR DC/DC CONVERTER

We compare the suggested converter to current topologies that have been employed in the past in this section. When evaluating converters, voltage gain, voltage stress on semiconductor devices, total device rating (TDR), common ground, and input current type are all taken into account. Figure 15 shows a comparison of the proposed converter's boosting capabilities. In all duty ratio ranges, the suggested converter with $n = 3$ has the maximum voltage gain of all the stated converters in Table 2. The suggested two-stage converter ($n = 2$) has the maximum

TABLE 2 Comparison with the similar DC/DC converters

Topology	Reactive Components		Semiconductor Components		Voltage Gain	Voltage Stress on Switch	Max. Voltage stress on diode	TDA (kVA)	Common Ground	Input Current type
	N_L	N_C	N_S	N_D						
TBC	1	1	1	1	$\frac{1}{1-k}$	v_o	v_o	4.5	✓	*Continuous*
TQBC	2	2	1	3	$\frac{1}{(1-k)^2}$	v_o	v_o	4.2	✓	*Continuous*
A	2	2	2	2	$\frac{2}{1-k}$	$\frac{v_o}{2}, v_o$	v_o	2.9	✓	*Continuous*
B	2	1	2	3	$\frac{1+k}{1-k}$	$\frac{v_o}{1+k}, v_o$	v_o	3.02	✓	*Continuous*
C	2	4	2	4	$\frac{4}{1-k}$	$\frac{v_o}{2}, \frac{v_o}{2}$	v_o	2.07	✓	*Continuous*
D	5	3	2	8	$\frac{1+5k+2k^2}{1-k}$	$\frac{(1+k)v_o}{1+5k+2k^2}$	–	–	✗	*Continuous*
E	3	4	2	5	$\frac{5+k}{1-k}$	$\frac{v_o}{5+k}, \frac{2v_o}{(5+k)}$	$\frac{3v_o}{(5+k)}$	1.54	✗	*Continuous*
F	4	3	2	7	$\frac{3+k}{1-k}$	$\frac{2v_o}{3+k}, \frac{(1+k)v_o}{3+k}$	v_o	3.23	✓	*Continuous*
G	2	5	1	6	$\frac{2(2-k)}{(1-k)^2}$	$\frac{v_o}{2}$	$\frac{v_o}{2}$	9.7	✗	*Continuous*
H	2	5	2	5	$\frac{5+k}{1-k}$	$\frac{v_o}{5+k}$	$\frac{2v_o}{5+k}$	1.55	✗	*Continuous*
I	3	3	1	3	$\frac{k}{(1-k)^2}$	v_o	$\frac{v_o}{k}$	5.7	✓	*Continuous*
J	3	2	2	3	$\frac{1+3k}{1-k}$	$\frac{v_o}{1+3k}$	$\frac{2v_o}{1+3k}$	0.66	✗	*Continuous*
Proposed (*dSIC-iVL*) *n=2*	2	6	1	7	$\frac{6}{1-k}$	$\frac{v_o}{3}$	$\frac{v_o}{3}$	1.74	✓	*Continuous*
Proposed (*nSIC-iVL*) *n=3*	2	8	1	9	$\frac{8}{1-k}$	$\frac{v_o}{4}$	$\frac{v_o}{4}$	1.8	✓	*Continuous*
Proposed (*nSIC-iVL*)	2	8	1	9	$\frac{2(n+1)}{1-k}$	$\frac{v_o}{(n+1)}$	$\frac{v_o}{(n+1)}$	-	✓	*Continuous*

N_L: Inductor Count, **N_C:** Capacitor Count, **N_S:** Switch Count, **N_D:** Diode Count, ✓: Yes, ✗: No
A: Shima Sadaf et al(2021) [11], **B:** Sadaf, S. et al(2021) [10], **C:** S. Sadaf et al(2021) [9], **D:** M. S. Bhaskar et al (2021) [12], **E:** Zaid et al (2021), [7] **F:** S. Khan et al (2021) [8], **G:** A. Mahmood et al (2021) [15], **H:** A. M. S. S. Andrade et al (2021) [13], **I:** P. K. Maroti et al (2019) [23], **J:** S. A. Ansari et al (2019) [24]

gain until $k = 0.5$, after which converter G has the highest gain owing to quadratic gain; however, the converter G has several drawbacks that will be detailed later in this section

Furthermore, the suggested converter incorporates an expandability feature that further boosts the voltage gain. A single switch is used in the dSIC-iVL converter, whereas two switches are used in converters A, B, C, D, E, F, and H. Two inductors equal to TQBC are used in the proposed dSIC-iVL converter, converters A, B, C, G, and H. Converters E, I, and J use three inductors, converter F has four inductors, and converter D has the most inductors; however, the dSIC-iVL converter has the maximum voltage gain. The suggested dSIC-iVL converter has the largest number of capacitors. Seven diodes make up the dSIC-iVL converter, which is the same as the converter F. The maximum number of diodes in the converter D is eight. The total number of components is highest in converter D, whereas the proposed dSIC-iVL converter and converter F have 16 components.

Attributed to the reason that voltage gain is not a sufficient criterion for evaluating the converter's performance, different devices were used to compare the converter. Figures 15 through 19 show the voltage gains per inductor count, switch count, diode count, and capacitor count. Other converters have the lowest voltage gain per inductor count and switch count. However, when the number of stages increases, the voltage gain per inductor and switch rises because only diodes and capacitors grow in number, while inductors and switches remain constant, as shown in Figures 16 and 17. The proposed converter has voltage gain per capacitor count equal to converter A, TBC, and C, as shown in Figure 18. The voltage gain per diode count is shown in Figure 19. It can be seen from the same figure that voltage gain per diode count is greater than converters B, D, I, and F.

The switch's voltage stress is critical for assessing DC/DC topologies. Figure 20 provides a graphical representation of the switch's normalized voltage stress. Of all the reported converters included in the comparison (Table 2), the suggested

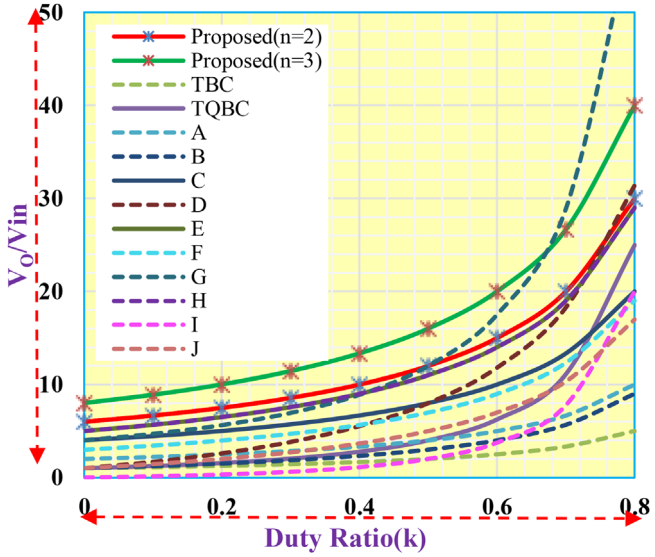

FIGURE 15 Voltage gain at different duty ratios

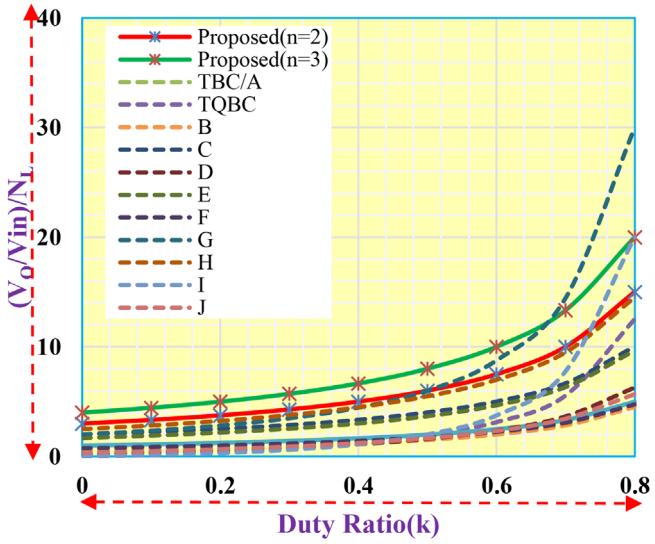

FIGURE 16 Voltage gain per inductor count at different duty ratios

converter has the lowest voltage stress on the switch. The normalized switch voltage stress in the proposed converter falls as the number of stages rises, as shown in Figure 20. In Figure 21, the maximum voltage stress on the diodes is also compared. In general, like the TBC, TQBC, converters A, B, C, and F, the output diode has voltage stress equal to the output voltage. The suggested converter eliminates this drawback. Among all the converters studied, the voltage stress on the diodes is the lowest. The normalized diode voltage stresses in the proposed converter decrease as the number of stages rises, as shown in Figure 21. Low voltage stress on semiconductor components reduces costs while increasing efficiency. The sum of the individual product of current and voltage ratings is the TDR. Table 2 shows how the TDR of all converters at 200 W is determined given the exact operational requirements. The proposed

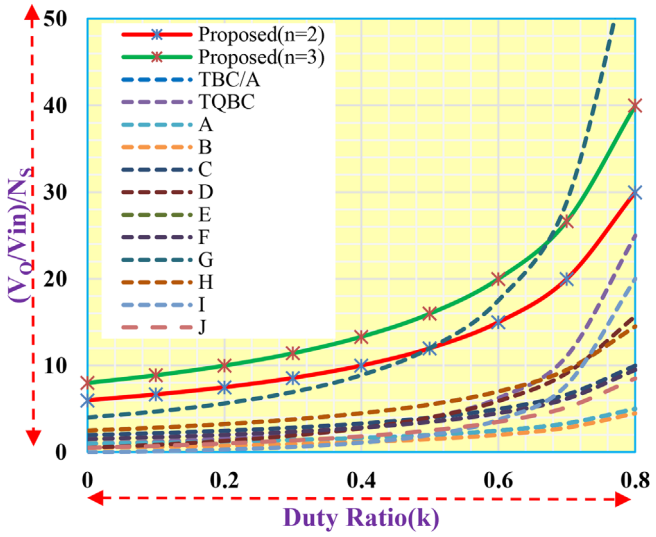

FIGURE 17 Voltage gain per switch count at different duty ratios

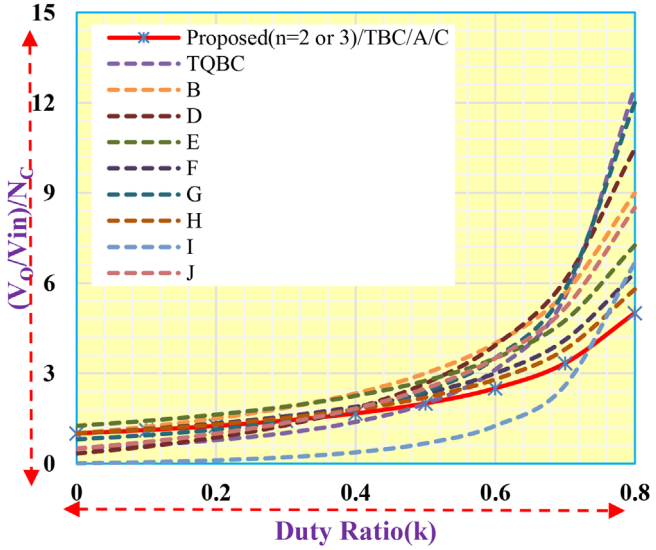

FIGURE 18 Voltage gain per capacitor count at different duty ratios

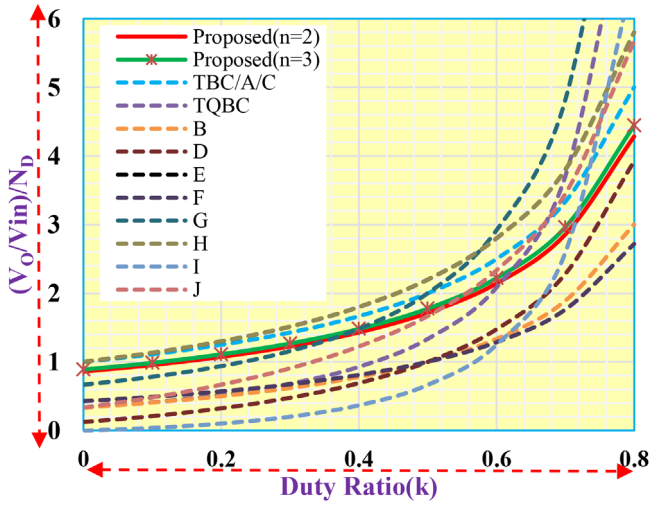

FIGURE 19 Voltage gain per diode count at different duty ratios

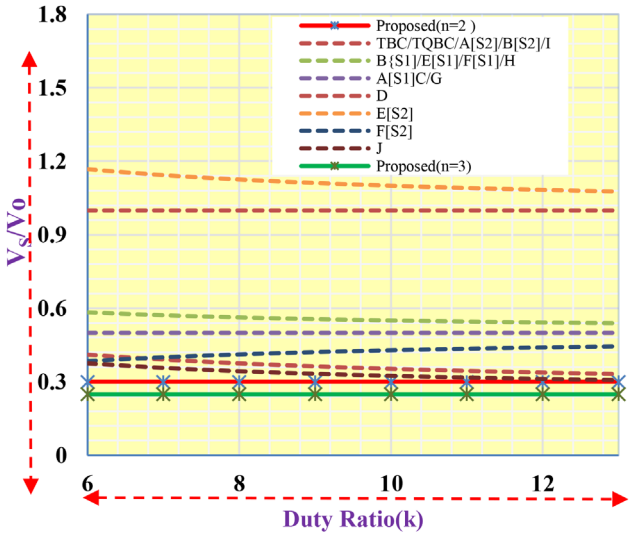

FIGURE 20 Normalized switch voltage stress at different voltage gain

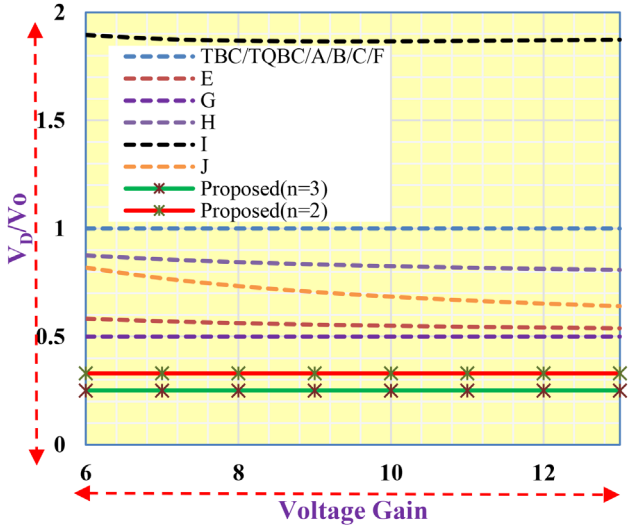

FIGURE 21 Normalized diode voltage stress at different voltage gain

converter has a lower TDR rating except for J, H, and E converters.

Unlike converters B, D, F, and I, the converter has a common connection between input and output, making it ideal for a broad range of applications. Furthermore, there is no extra *dv/dt* between the input and output grounds. The converter is suited for MPPT applications because it has a continuous input current. As a result, it can be stated that the suggested converter outperforms the other converters in terms of voltage gain, voltage stress on semiconductor devices, total device rating, common ground connection between source and load, and converter expandability.

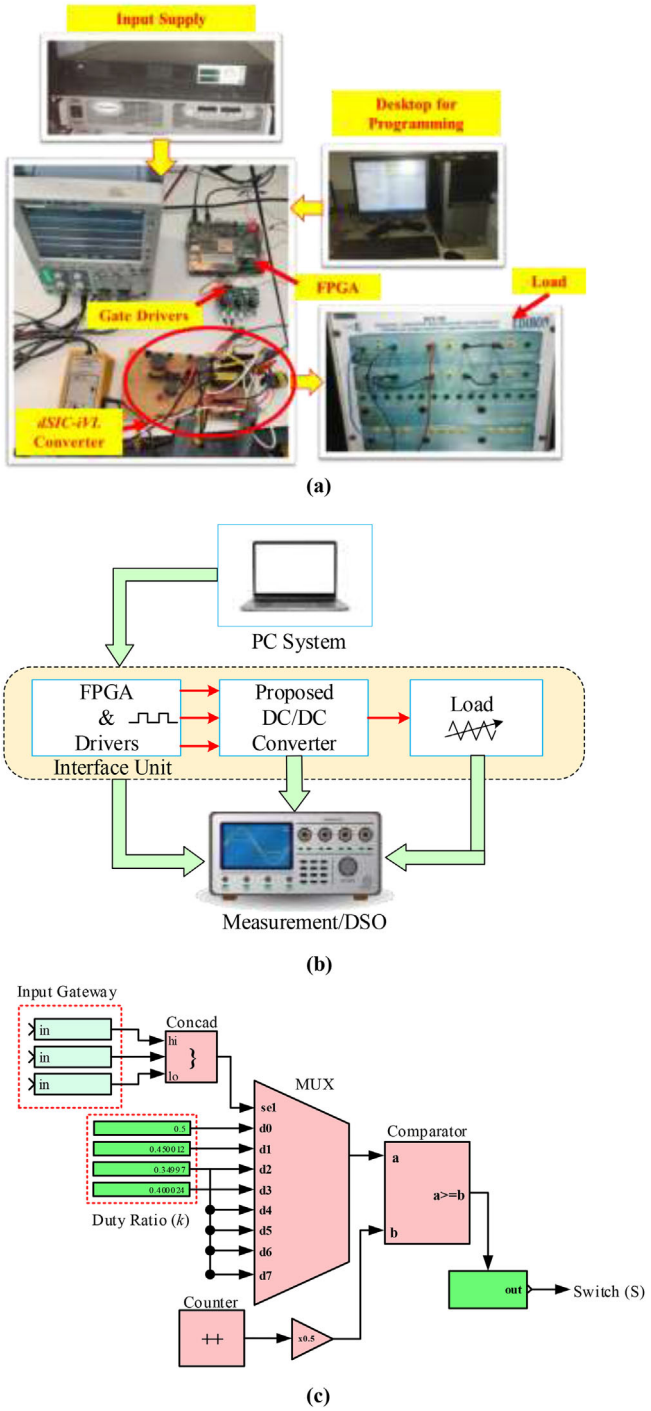

FIGURE 22 (a) Experimental setup of dSIC-iVL converter. (b) Block diagram of the proposed converter. (c) Block diagram of switching pulse generation scheme

9 | EXPERIMENTAL RESULTS DISCUSSION IN CCM MODE

This subsection determines the actual world performance evaluation of the double-stage dSIC-iVL converter. Figure 22a shows the hardware prototype, with specifications listed in Table 3. PWM gate signals are generated by an FPGA Vertix-5

TABLE 3 Hardware specifications of the converter

Parameter	Value
Input supply	20 V
Switching frequency	50 kHz
Inductor L_{Z1}, L_{Z2}	1 mH
Capacitors	C_o = 220 μF, 450 V $C_{Z1//1/2/3/4}$ = 220 μF, 250 V
Switches	C3M0065090, r_{ON} = 10 mΩ, 900 V, 36 A
Diodes	STTH30R04, V_{RRM} = 400 V, V_F = 0.4 V, r_{ON} = 0.01 Ω, I_F = 30 A
Controller	FPGA Vertix-5 (XC5VLX50T)
Driver	GDX-4A22S1
Load resistance	400 Ω

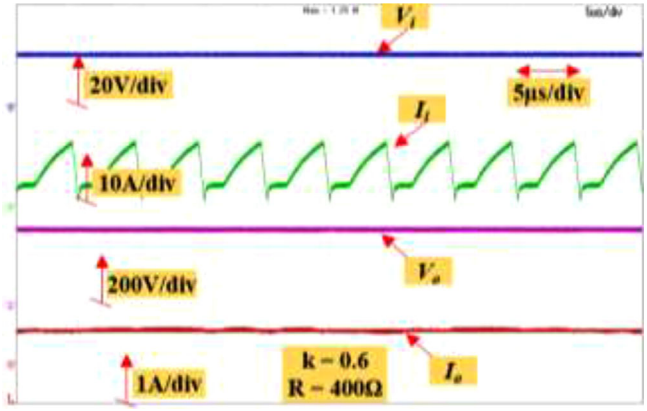

FIGURE 23 Top to bottom: experimental waveforms of input supply voltage, input current, output voltage, and output load current at duty ratio equal to 0.6

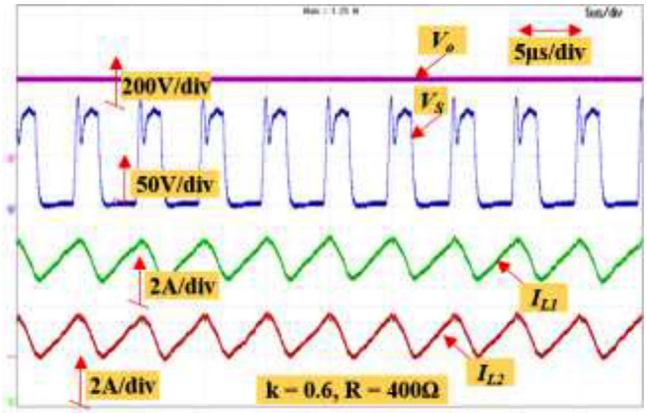

FIGURE 24 Top to bottom: experimental waveforms of the output voltage, drain to source switch voltage, current of inductor L_1, and current of inductor L_2 at duty ratio equal to 0.6

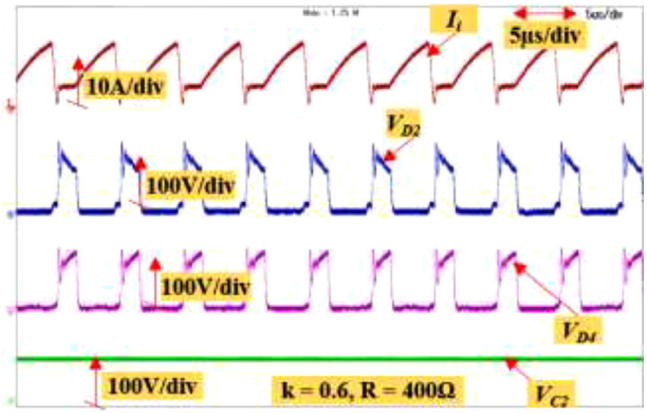

FIGURE 25 Top to bottom: experimental waveforms of input current, diode D_2 voltage, diode D_4 voltage, and capacitor C_2 voltage at duty ratio equal to 0.6

(XC5VLX50T) controller to control the power switches externally. In addition, as illustrated in Figure 22b, a driver circuit GDX-4A22S1 is used to increase the gate signal to the requisite level to trigger the MOSFETS.

The block diagram of the proposed converter and the block diagram of the control technique to generate the gate pulse are shown in Figures 22b and 22c, respectively. A MUX, comparator, logic gate, constant, and counter block are used to create the switching pulses. To create the PWM pulse for the switch (S), a counter block generates the carrier waveform (sawtooth) and compares it to the output of MUX.

The input supply is set to 20 V, and MOSFET is controlled with a gate pulse of 60%, as shown in Figure 23. The steady-state output voltage (V_o), load current (I_o), and input current (I_i) are captured in the same figure and are equal to 299 V, 0.74 A, and the continuous input current is observed with a load resistance of 400 Ω. The dip in the V_o from the ideal value is due to the non-ideal behaviour of the components. However, the input current is pulsating in nature with high ripple content. The converter can achieve a boosting factor of 14.95 under these circumstances.

With a fixed duty ratio of 60% and a load resistance of 400 Ω, the switch voltage (V_{ds}), currents of inductor L_1 (I_{L1}) and L_2 (I_{L2}) waveform are captured in Figure 24. In the same figure, the inductor currents I_{L1} and I_{L2} rise when the switch voltage across the switch is near zero. The inductor's currents rise from 4.5 A to a peak value of 6 A. When the switch is *OFF*, it blocks a voltage of 100 V, which is precisely one-third of the output voltage (V_O = 299 V). The inductor currents decrease from the peak value of 6 A to an initial value of 4.5 A. The average inductor current is observed equally to 5.62 A. The percentage of inductor current ripple observed is 22%.

The diodes D_2, D_4, and D_{Z1} are reverse biased when the switch is *OFF*, as shown in Figure 25. The peak reverse-biased voltage of D_2 and D_4 is observed near 100 V, which is approximately 33% of the output voltage. In Figure 26, the reverse-biased voltage of diode D_{Z1} is 50 V. When the switch is *ON*, the output diode D_0 is reversed biased, the peak voltage of the output diode is 100 V, one-third of the output voltage, and the capacitor C_4 voltage is 100 V.

When the duty ratio (k) is changed from 60% to 70%, with a fixed input supply of 20 V and load resistance, the output volt-

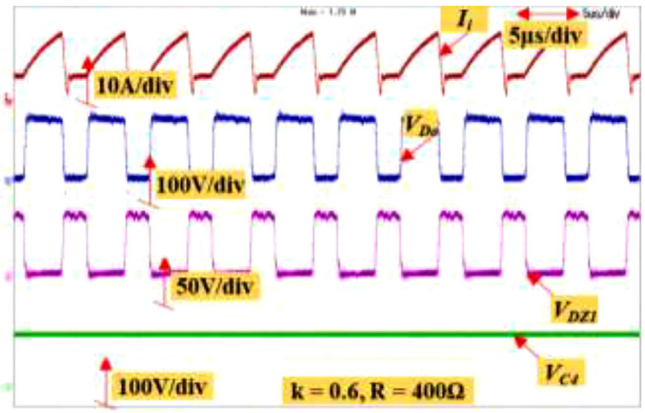

FIGURE 26 Top to bottom: experimental waveforms of input current, output diode D_0 voltage, diode D_{Z1} voltage, and capacitor C_4 voltage at duty ratio equal to 0.6

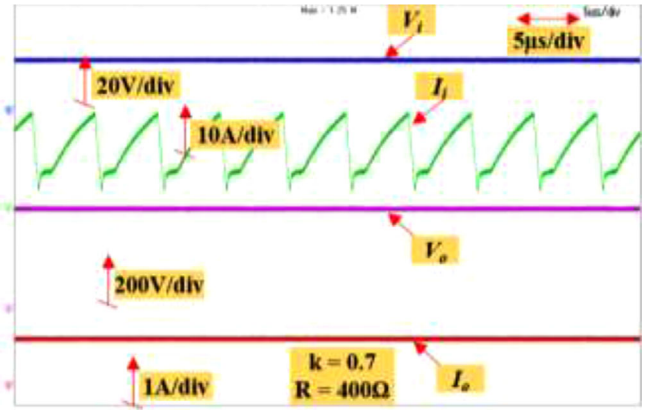

FIGURE 27 Top to bottom: experimental waveforms of input supply voltage, input current, output voltage, and output load current at duty ratio equal to 0.7

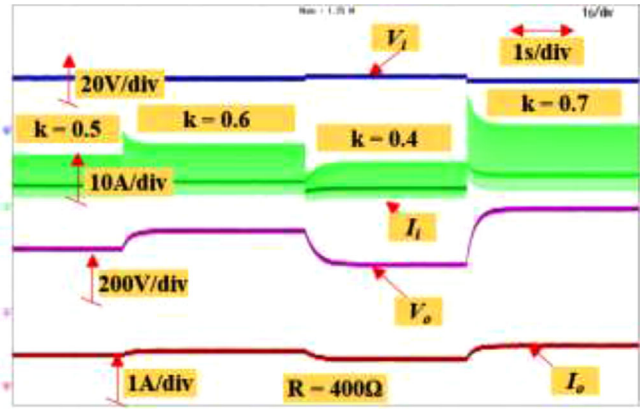

FIGURE 28 Top to bottom: experimental waveforms of Input voltage supply, input current, output voltage, and output load current with the dynamic change in duty ratio

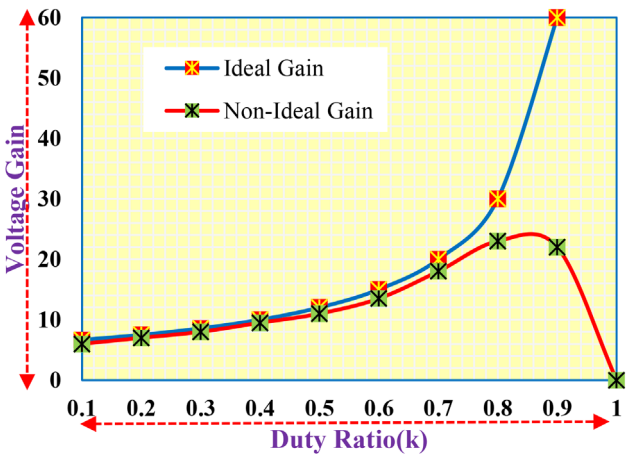

FIGURE 29 Ideal and experimental voltage gain

age increases to 398 V, as captured in Figure 27; it can also be observed that there is an increase in the load current near 1 A. The input current is also increased but is continuous in nature. The converter performance is also examined in dynamic conditions by changing the duty ratio at different levels with a constant load resistance of 400 Ω and maintaining input supply at 20 V. The step change in the duty ratio from 50% to 60% increases the output voltage from 240 to 299 V. The output load current is changed correspondingly from 0.6 to 0.75 A. The input current also increases, as seen from Figure 28. The duty ratio decreases to 0.4; the output voltage decreases to 200 V, the load current decreases to 0.5 A, and the input current decreases. Further, the duty ratio is increased to 70%, the output voltage is increased to 398 V, the load current is increased to 1 A, and the input current is increased (Figures 29, 30, and 31)

The actual voltage gain is represented in Fig. 29. The deviation is seen since the real model of the converter will have parasitic resistance in inductors, diodes, switches and capacitors and forward voltage drop in the power diodes. The percentage experimental efficiency of the converter is plotted in Fig. 30 at different output power levels. As the output power is increased the efficiency first increased and reaches a maximum value near 96% and then decreases at higher output power levels. The converter efficiency at 200W output power is 92%. The loss distribution among the components is shown in Fig. 31. The maximum loss is occurring in the diodes equal to 40% of the total loss i.e. 18.62W. The percentage of loss in the inductors is 30%, switch loss is 18% and losses occurring in the capacitors is equal to 12%.

10 | CONCLUSION

The proposed converter originated using switched inductor and improved voltage lift technique. The converter has fixed two inductors and a single switch. The converter has a number of benefits, including ultra-high voltage gain, low-voltage stress on switches and diodes, including the output diode, continuous input current, common ground connection between source and load, and the ability to expand into *n*-stages (nSIC-iVL) with fixed two inductors and a single power switch. The control is simple at all levels thanks to the single switch. When the

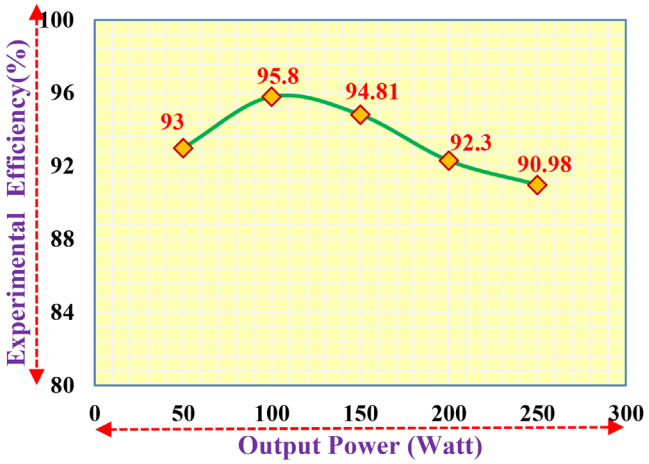

FIGURE 30 Experimental efficiency at different output power levels

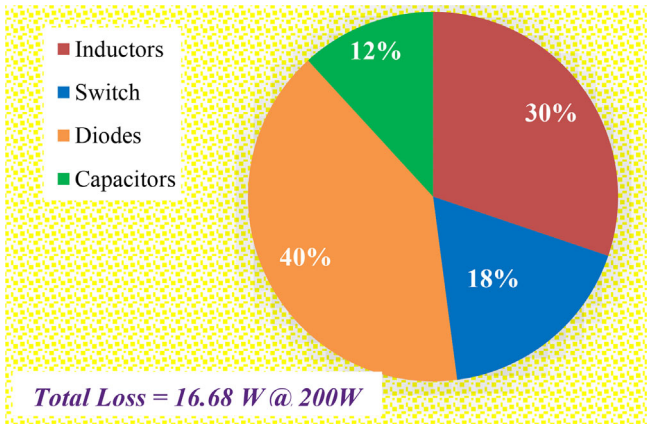

FIGURE 31 Percentage of loss occurring in components at 200 W

converter stages are raised, the output voltage acquired forms a series in an increasing arithmetic progression. In addition, as the number of stages increases, the voltage stress on semiconductors decreases. The steady-state analysis was investigated in CCM, DCM, and boundary condition mode. Non-ideal analysis, component power loss, efficiency, and non-ideal voltage were all examined. The proposed converter was compared with recent DC/DC converters; the voltage gain per inductor count, diode count, and switch count was significantly high. The switch voltage stress and diode voltage stress are lower than recent converters. The total device rating was lower than the recent converters. The input current was pulsating in nature with high ripple content, which sets a limitation to the proposed converter. A 250 W hardware prototype was tested for various power ratings, and the highest efficiency was discovered to be 95.8%. The converter's performance under dynamic conditions was found to be satisfactory, and experimental findings were found to be in good accordance with theoretical results. The converter is transformerless and belongs to the non-isolated group. As a result, the converter is a good fit for high-voltage applications.

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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