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Modulation With Metaheuristic Approach for Cascaded-MPUC49 Asymmetrical Inverter With Boosted Output

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ABSTRACT This work introduces a 49-level Asymmetrical Inverter (AMLI) with boosted output based on the cascaded operation of two 7-Level Modified Packed U-Cell inverters (MPUC-7). The converter is capable of operation with a boosted voltage of up to 1.714 times the maximum DC voltage employed. It requires only 12 active switches and 4 voltage sources. With the sources set in the ratio of 14 : 7 : 2 : 1, the 7-level output of the two converters is so utilized that the $7^2 = 49$ -level output voltage is generated across the load. A detailed explanation of level formation is discussed. This converter is operated using an Artificial Neural Network (ANN) which is trained for the harmonic elimination in the output voltage waveform. For the calculation of optimum angles, a meta-heuristic based Genetic Algorithm (GA) technique is employed. The generation of 49-level output requires 24 transitions in one quarter of a cycle. All these angles are generated for various desired output voltages, and the ANN is trained offline for the same. The converter and its control are simulated in MATLAB/Simulink[®] environment, and the results are verified on the experimental setup. The multilevel output thus obtained is nearly sinusoidal and the Total Harmonic Distortion (THD) thus produced is under the specified limit of IEEE.

INDEX TERMS MPUC-7 converter, cascaded operation, boosted output voltage, genetic algorithm, harmonic elimination, artificial neural network.

I. INTRODUCTION

Multilevel Inverters (MLIs) have shown their efficacy in medium and high power applications due to better quality output waveforms, low rating switches, and several other factors, and thus pose as a replacement technology to the conventionally employed 2-level inverters. The main advantage of MLIs is the ability to synthesize voltages of low harmonic content. MLIs are broadly classified into symmetrical and asymmetrical topologies based on the voltage sources employed. If the sources are of the same value, then the configuration will fall under symmetrical category;

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else, it will be asymmetrical. Symmetrical multilevel Inverters (SMLI) have been explored exhaustively in the literature since their introduction as Neutral Point Clamped MLI (NPMLI) in 1981 [1], as Flying Capacitor MLI (FCMLI) in 1992 [2], and, as classical cascaded H-Bridge (CHBMLI) inverter in 1996 [3]. These configurations were based on the concept of synthesizing the stepped waveforms of higher voltage levels from various DC sources of lower ratings. Diode Clamped (DCMLI) or FCMLI topologies employ a large number of switching devices, diodes and capacitors. On the other hand, the CHBMLI topology seems to be a promising one, but suffers from employment of a large number of DC sources and switches. Asymmetric Multilevel Inverters (AMLI), on the other hand, employ voltage

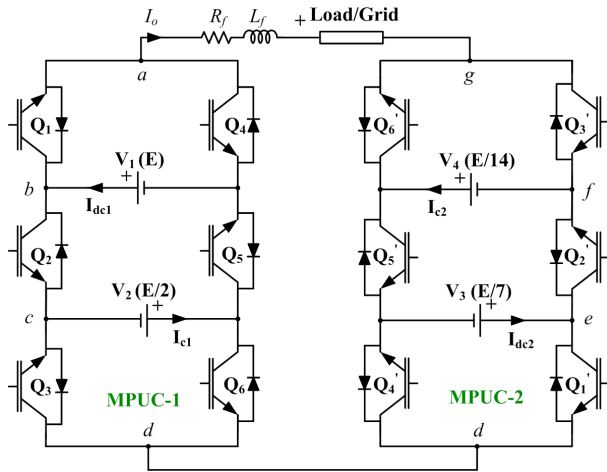


FIGURE 1. A cascaded MPUC to produce 49-level output voltage.

sources of different ratings, and are gaining popularity over the conventional symmetrical topologies. One such topology is the Packed U-cell (PUC) [4], which has shown some promising results with fewer switching devices and a single power supply. For instance, for a 7-level voltage profile in a single-phase operation, FCMLI employs twelve switches and six capacitors; CHBMLI employs twelve switches and three DC sources; whereas, the PUC employs six switches, one DC source and one capacitor. This accounts for a dramatic difference in terms of cost, complexity, reliability and losses. A detailed review on SMLI and AMLI is contained in [5].

The basic topology of PUC was introduced in [6] as a modification to CHBMLI with two DC sources. Later in [4], this topology was converted into a single voltage source (forming the main DC-link) and one capacitor (forming the auxiliary DC-link) topology that can generate five or seven levels, depending on the DC-link to auxiliary DC-link voltage ratio. The hysteresis control of this converter producing a 7-level output voltage is considered in [7]. Six bands on the inverter output voltage–output current curve are utilized to control the output currents. Through the addition of one more cell, this topology is able to produce fifteen levels, as shown in [7]. Its effectiveness as a potential DC-AC as well as AC-AC converter is shown in [8]. Model predictive control (MPC) was applied on PUC in [9] to regulate the auxiliary DC-link voltage at the desired voltage level of $V_{dc}/3$, so as to achieve the 7-level operation, simultaneously monitoring the active and reactive power flow by controlling the current flowing at the point of coupling of the converter and the grid. A sensorless control, in which the voltage of the auxiliary DC-link is regulated without the usage of a voltage sensor, is proposed for a 5-level PUC in [10], which is also extended to a 15-level PUC in [11]. A proportional resonant controller is designed for a 5-level PUC with an appropriate filter design for grid connection in [12]. Trabelsi in [13] has explored the finite control set MPC for the grid connected 7-level PUC. Evaluation of level-shifted and phase-shifted PWM (Pulse Width Modulation) techniques for a 7-level PUC is

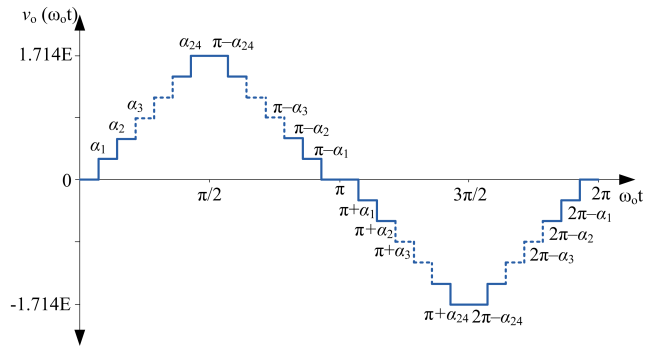


FIGURE 2. Proposed output voltage levels of MPUC49 level inverter.

presented in [14]. A novel and less complex modulation strategy in which sensorless control of auxiliary DC-link voltage employs only two carriers is presented in [15]. An improved PUC is discussed in [16], wherein a 5-level PUC is enhanced to a 7-level PUC with boosted output voltages to $1.5 V_{dc}$, by addition of three more switches to the existing topology. Harmonics are minimized in the output voltage of a 5-level PUC by employing the modified angles which are obtained by genetic algorithm (GA) [17]. A modified PUC (MPUC) was introduced in [18], which was able to generate 7-level output voltage whose magnitude was more than the DC-link value.

Converters with a large number of output levels by cascading operation are being discussed. One such example is contained in [19]. This cascading operation requires 4 DC source and produces 31-level output. Recently, a 49-level AMLI was proposed by cascading two PUCs [20], in which two asymmetrical batteries and two capacitors were employed. These 49 levels were achieved by employment of 2 DC sources and 12 IGBTs only. In this structure, one of the PUC was modulated at high switching frequency, while the other was modulated at low switching frequency in step mode, thus enabling operation in a variable frequency control mode. The cascading of a 7-level PUC with DC link voltage ratio at 1 : 7 and the corresponding auxiliary DC-link voltage at the ratio of 1 : 3, will produce a 49-level output voltage. A detailed discussion on such cascaded PUCs is contained in [21]. Other AMLIs are presented in [22]–[26].

This work discusses the cascaded operation of a MPUC where the THD (Total Harmonic Distortion) in the output voltage is reduced by mitigating the major harmonic content by calculating the switching angles using a metaheuristic approach. Metaheuristic approaches are now being extensively employed in power electronic control algorithms [27]. The method applied here is the Genetic Algorithm (GA), which is a search based algorithm that is employed to find solutions to the optimization problems where it is difficult to find an extrema through generalized differential calculus – either due to nonlinear structure of the problem, or due to its complexity. The advantages of this method are a guaranteed convergence (provided that the objective function is correctly defined), and its simplicity [17]. An Artificial Neural

Network (ANN) based controller is then employed which generates the optimum switching signals, and is trained according to the solutions obtained from the GA-based algorithm. Some of the applications of ANN in power electronics control can be seen in [28], [29]. The advantages of the 49-level inverter employed in this paper over the inverter discussed in [20] is that this converter produces a boosted voltage of 1.714 times the maximum voltage employed in the circuitry, which is 1.5 times the voltage achieved earlier. Moreover, the voltage ratios of both the converters suggest that for same voltage output, the DC voltage source of low value will be employed in this inverter.

The paper proceeds as follows. Firstly, the cascaded operation of PUCs and the corresponding generation of 49-levels is discussed. Then the expressions are developed that describe the angles of level transition. In section IV, GA-based optimization is discussed and implemented to determine the optimum angles that will result in the mitigated output voltage. In the fifth section, the ANN-based controller is discussed, whose optimal weights are derived according to the angles achieved in the section IV. Finally, the results are verified by simulation in the MATLAB/SIMULINK[®] environment and on a 1 kW experimental setup.

II. 49-LEVEL OPERATION OF CASCADED MPUC

The Cascaded MPUC (CMPUC) inverter, represented in Fig. 1, is obtained by slight modifications of the cascaded PUC inverter [20]. Cascading of the MPUC inverter has a multiplicative effect, that results in a significant increase in output voltage levels. In order to obtain higher voltage levels, one solution is to modify the traditionally used inverters and the other solution can be cascading (as performed by the authors here). Cascading results in a large number of voltage levels, with minimal use of switches. In CMPUC, in order to obtain 49 levels, the constraint on the choice of input side voltages is given by (1):

$$V_1 = 2V_2 = 7V_3 = 14V_4 \quad (1)$$

where V_1 and V_3 are the primary DC link voltages and V_2 and V_4 are the corresponding auxiliary voltage levels respectively. The main feature of this configuration is the ability to boost the voltage more than the maximum DC magnitude available, which is contrasted with the CPUC49 discussed in [20]. The maximum voltage that is achievable is:

$$V_o^{\max} = \frac{24}{14}E = 1.714E \quad (2)$$

where, E is the magnitude of the highest voltage source.

The CMPUC inverter comprises anti-parallel switches (Q_1 and Q_4 , Q_2 and Q_5 , Q_3 and Q_6 , $Q_{1'}$ and $Q_{4'}$, $Q_{2'}$ and $Q_{5'}$, and $Q_{3'}$ and $Q_{6'}$). The anti-parallel switches work in complementary mode (i.e. no two anti-parallel switches are turned on simultaneously). The output voltage levels of the CMPUC inverter are listed in table 1. The switching operation of the

TABLE 1. Switching States of 49-Level PUC Inverter.

State	Q_1	Q_2	Q_3	$Q_{1'}$	$Q_{2'}$	$Q_{4'}$	$V_1 + V_{II}$	V_o
1.	0	0	0	0	0	0	0 + 0	0
2.	0	0	0	0	0	1	0 + V_4	$E/14$
3.	0	0	0	0	1	0	0 - ($V_3 + V_4$)	$-3E/14$
4.	0	0	0	0	1	1	0 - V_3	$-2E/14$
5.	0	0	0	1	0	0	0 + V_3	$2E/14$
6.	0	0	0	1	0	1	0 + ($V_3 + V_4$)	$3E/14$
7.	0	0	0	1	1	0	0 - V_4	$-E/14$
8.	0	0	0	1	1	1	0 + 0	0
9.	0	0	1	0	0	0	$V_2 + 0$	$7E/14$
10.	0	0	1	0	0	1	$V_2 + V_4$	$8E/14$
11.	0	0	1	0	1	0	$V_2 - (V_3 + V_4)$	$4E/14$
12.	0	0	1	0	1	1	$V_2 - V_3$	$5E/14$
13.	0	0	1	1	0	0	$V_2 + V_3$	$9E/14$
14.	0	0	1	1	0	1	$V_2 + (V_3 + V_4)$	$10E/14$
15.	0	0	1	1	1	0	$V_2 - V_4$	$6E/14$
16.	0	0	1	1	1	1	$V_2 + 0$	$7E/14$
17.	0	1	0	0	0	0	$-(V_1 + V_2) + 0$	$-21E/14$
18.	0	1	0	0	0	1	$-(V_1 + V_2) + V_4$	$-20E/14$
19.	0	1	0	0	1	0	$-(V_1 + V_2) - (V_3 + V_4)$	$-24E/14$
20.	0	1	0	0	1	1	$-(V_1 + V_2) - V_3$	$-23E/14$
21.	0	1	0	1	0	0	$-(V_1 + V_2) + V_3$	$-19E/14$
22.	0	1	0	1	0	1	$-(V_1 + V_2) + (V_3 + V_4)$	$-18E/14$
23.	0	1	0	1	1	0	$-(V_1 + V_2) - V_4$	$-22E/14$
24.	0	1	0	1	1	1	$-(V_1 + V_2) + 0$	$-21E/14$
25.	0	1	1	0	0	0	$-V_1 + 0$	$-14E/14$
26.	0	1	1	0	0	1	$-V_1 + V_4$	$-13E/14$
27.	0	1	1	0	1	0	$-V_1 - (V_3 + V_4)$	$-17E/14$
28.	0	1	1	0	1	1	$-V_1 - V_3$	$-16E/14$
29.	0	1	1	1	0	0	$-V_1 + V_3$	$-12E/14$
30.	0	1	1	1	0	1	$-V_1 + (V_3 + V_4)$	$-11E/14$
31.	0	1	1	1	1	0	$-V_1 - V_4$	$-15E/14$
32.	0	1	1	1	1	1	$-V_1 + 0$	$-14E/14$
33.	1	0	0	0	0	0	$V_1 + 0$	$14E/14$
34.	1	0	0	0	0	1	$V_1 + V_4$	$15E/14$
35.	1	0	0	0	1	0	$V_1 - (V_3 + V_4)$	$11E/14$
36.	1	0	0	0	1	1	$V_1 - V_3$	$12E/14$
37.	1	0	0	1	0	0	$V_1 + V_3$	$16E/14$
38.	1	0	0	1	0	1	$V_1 + (V_3 + V_4)$	$17E/14$
39.	1	0	0	1	1	0	$V_1 - V_4$	$13E/14$
40.	1	0	0	1	1	1	$V_1 + 0$	$14E/14$
41.	1	0	1	0	0	0	$(V_1 + V_2) + 0$	$21E/14$
42.	1	0	1	0	0	1	$(V_1 + V_2) + V_4$	$22E/14$
43.	1	0	1	0	1	0	$(V_1 + V_2) - (V_3 + V_4)$	$18E/14$
44.	1	0	1	0	1	1	$(V_1 + V_2) - V_3$	$19E/14$
45.	1	0	1	1	0	0	$(V_1 + V_2) + V_3$	$23E/14$
46.	1	0	1	1	0	1	$(V_1 + V_2) + (V_3 + V_4)$	$24E/14$
47.	1	0	1	1	1	0	$(V_1 + V_2) - V_4$	$20E/14$
48.	1	0	1	1	1	1	$(V_1 + V_2) + 0$	$21E/14$
49.	1	1	0	0	0	0	$-V_2 + 0$	$-7E/14$
50.	1	1	0	0	0	1	$-V_2 + V_4$	$-6E/14$
51.	1	1	0	0	1	0	$-V_2 - (V_3 + V_4)$	$-10E/14$
52.	1	1	0	0	1	1	$-V_2 - V_3$	$-9E/14$
53.	1	1	0	1	0	0	$-V_2 + V_3$	$-5E/14$
54.	1	1	0	1	0	1	$-V_2 + (V_3 + V_4)$	$-4E/14$
55.	1	1	0	1	1	0	$-V_2 - V_4$	$-8E/14$
56.	1	1	0	1	1	1	$-V_2 + 0$	$-7E/14$
57.	1	1	1	0	0	0	0 + 0	0
58.	1	1	1	0	0	1	0 + V_4	$E/14$
59.	1	1	1	0	1	0	0 - ($V_3 + V_4$)	$-3E/14$
60.	1	1	1	0	1	1	0 - V_3	$-2E/14$
61.	1	1	1	1	0	0	0 + V_3	$2E/14$
62.	1	1	1	1	0	1	0 + ($V_3 + V_4$)	$3E/14$
63.	1	1	1	1	1	0	0 - V_4	$-E/14$
64.	1	1	1	1	1	1	0 + 0	0

CMPUC is defined by:

$$Q_i = \begin{cases} 0 & \text{if } Q_i \text{ is off} \\ 1 & \text{if } Q_i \text{ is on} \end{cases} \quad i = 1, 2, 3, 1', 2', 3' \quad (3)$$

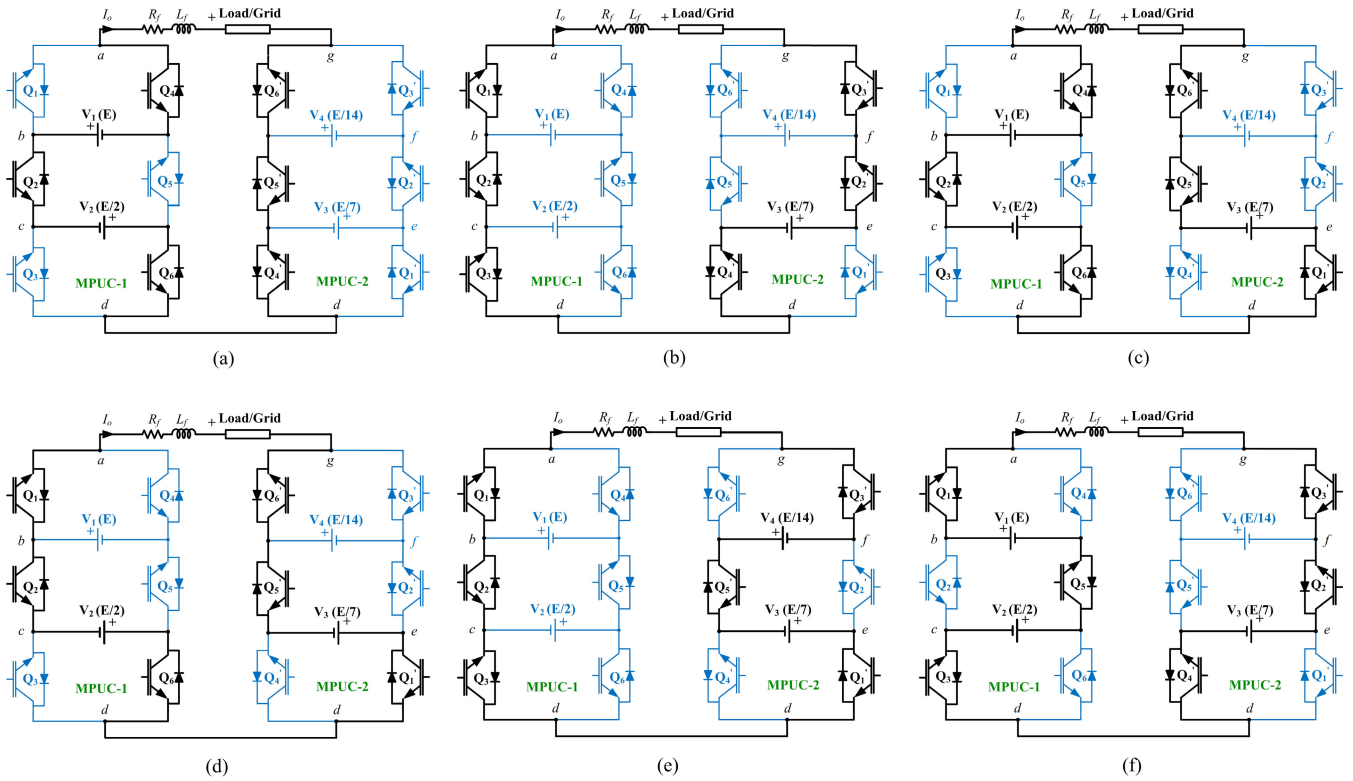


FIGURE 3. Illustration of few states of the cascaded MPUC.

The output voltage (V_o) of the converter is defined as:

$$V_o = V_{ab} + V_{bc} + V_{cd} + V_{de} + V_{ef} + V_{fg} \quad (4)$$

where, the points a, b, c, d, e, f and g are shown in Fig. 1. The output voltage in terms of switching function is established as:

$$\left. \begin{aligned} V_{ab} &= (Q_1 - 1) V_1 \\ V_{bc} &= (1 - Q_2) (V_1 - V_2) \\ V_{cd} &= (1 - Q_3) V_2 \\ V_{de} &= (Q_1' - 1) V_3 \\ V_{ef} &= (1 - Q_2') (V_3 - V_4) \\ V_{fg} &= (1 - Q_3') V_4 \end{aligned} \right\} \quad (5)$$

Thus, V_{ag} or V_o can be calculated as;

$$V_o = V_1 Q_1 + (V_2 - V_1) Q_2 - V_2 Q_3 + V_3 Q_1' + (V_4 - V_3) Q_2' - V_4 Q_3' \quad (6)$$

All the states of the converter, of which the descriptive waveform is shown in Fig. 2, are shown in Table 1. Some of the states are shown in Fig. 3.

III. SHM IN 49-LEVEL PUC

In Selective Harmonic Elimination (SHE), the energy of the low-order harmonics (that are omitted) is transferred to the higher-order harmonics, and thus the harmonics are not removed but replaced. Thus, it is better to opt for Selective Harmonic Mitigation (SHM) in which the harmonic content is minimized without the energy being transferred to higher frequency zone.

A. BASIC WAVEFORM AND THD ANALYSIS

The proposed 49-level waveform of the inverter shown in Fig 2 can be written as a combination of the step functions:

$$V(t) = E \left[\sum_{m=1}^{24} u(t - \alpha_m) - \sum_{m=1}^{24} u(t - (\pi - \alpha_m)) + \sum_{m=1}^{24} u(t - (\pi - \alpha_m)) + \sum_{m=1}^{24} u(t - (2\pi - \alpha_m)) \right] \quad (7)$$

As the waveform displays half-wave and quarter-wave symmetry, the Fourier expansion of the waveform will only contain odd harmonics, whose amplitude is represented as:

$$V_n = \frac{2}{T_o} \int_{t_o} V(t) \sin(n\omega_o t) dt \quad \forall n = 1, 3, 5, \dots \quad (8)$$

Putting $V(t)$ from (7) in the above equation will lead to:

$$V_n = \frac{4}{n\pi} \left[\sum_{m=1}^{24} E \cos(n\alpha_m) \right] \quad (9)$$

where, $V_1 < V_3 < \dots < V_{49}$, and $\alpha_1 < \alpha_2 < \dots < \alpha_{24}$.

The Total harmonic distortion can be calculated by:

$$THD = \frac{\sqrt{\sum_{n=3,5,\dots}^{\infty} \left[\frac{4E}{n\pi} \sum_{i=1}^{24} \cos(n\alpha_i) \right]^2}}{\frac{4E}{\pi} \left[\sum_{i=1}^{24} \cos(\alpha_i) \right]} \quad (10)$$

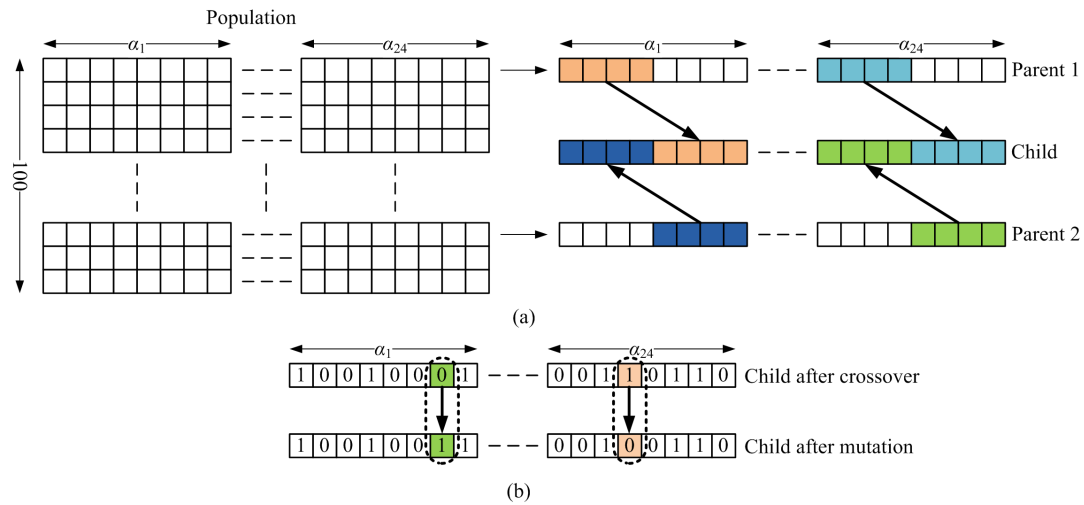


FIGURE 4. Steps of GA: (a) Crossover and (b) Mutation.

B. THE OBJECTIVE FUNCTION

The controller is designed in two stages. First, the equations discussed below are solved by Genetic Algorithm (GA) resulting in the solution of angles that ideally should reduce the magnitude of harmonic content up to 49th order to zero. This requires the formation of a fitness function for GA in terms of harmonic equations. Taking V_m as the magnitude of the fundamental voltage required, the expression can be written as:

$$\frac{\sqrt{2}V_m\pi}{4} - \left[\sum_{m=1}^{24} \frac{mE}{14} \cos(\alpha_m) \right] = 0 \quad (11)$$

and thus the fitness function f required for to be optimized is expressed as:

$$f(\alpha_1, \alpha_2, \dots, \alpha_{24}) = k_1|V_1 - V_m| + k_3|V_3| + \dots + k_{49}|V_{49}| \quad (12)$$

where, k_1, k_2, \dots, k_{49} are the weighted constants, with $k_1 > k_2 > \dots > k_{49}$.

IV. GENETIC ALGORITHM

Metaheuristic approaches have shown their efficacy in solving real-world optimization problems that are inherently non-linear and their convergence with conventional techniques either consume a lot of time or do not occur at all. Nature-inspired evolutionary techniques have evolved and are being implemented in a myriad of optimization applications. In this paper, a Genetic Algorithm (GA) is utilized to minimize the objective function that is derived in (12). The beneficial features of GA are: (i) the convergence is guaranteed (with certain tolerance band) and, (ii) the knowledge of derivatives is not required (as the iterations proceed with input-output mapping). The necessary steps are discussed in the following subsections and are supported by a detailed flowchart.

A. STEPS

1) DESIGN VARIABLES

The angles exhibited in Fig. 4 (from α_1 to α_{24}) are the same angles in (12). These angles form the variables and are to be corroborated in a manner defined in Fig. 2. For that a random population of 100 chromosomes is generated. Each chromosome is formed by 24 bytes, thus forming a length of $24 \times 8 = 192$ bits. The selection of the initial population is purely random. The weighted constants k_1, k_3, \dots, k_{49} are such defined that $k_1 > k_3 > \dots > k_{24}$, with $k_1 = 1000$. This prioritizes the harmonics that are to be eliminated.

2) SELECTION

The next step after the population is initialized, is to select two random parents on a purely probabilistic basis. In this paper the approach is based on the Roulette wheel criteria. The random selection of the parents ensures greater exploration of the solution domain. This also reflects in the results as a sudden surge, as shown in Fig. 6(b).

3) CROSSOVER

The crossover means blending of the genes in a particular manner. In this work the child's chromosome is formed by taking half of the bits from the first parent and the other half from the spouse. This is done for the whole 24 bytes of the chromosomes, as is exhibited in Fig. 4(a). N such children are produced, where ϵ is the current child as shown in Fig. 5.

4) MUTATION

Mutation basically defines the improvement in the child over the parent's behavior. So, in GA algorithms, this is achieved by flipping the values of the bits. Here, a single bit of each byte of the child's chromosome is changed, as exhibited in Fig. 4(b). Furthermore, it is ensured that the whole children population is not mutated. Instead, a random number μ is generated, and, if its value is less than a fixed number M (here 0.2), then only the child will be mutated. This is shown in Fig. 5.

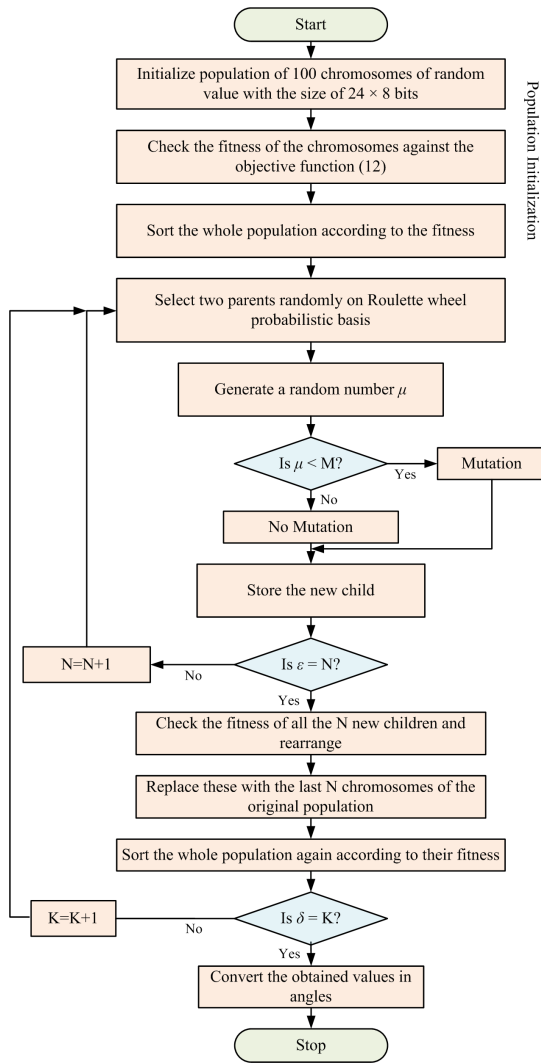


FIGURE 5. Flowchart of implementation of GA Algorithm.

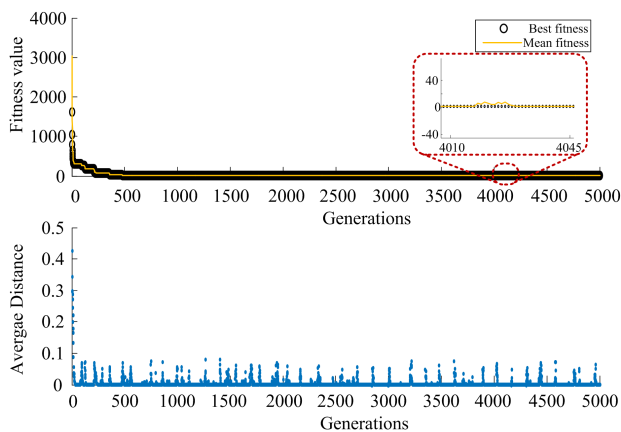


FIGURE 6. Convergence to the best solution, according to (a) fitness, and (b) according to the average distance from the mean value.

B. METHODOLOGY

The population is arranged according to their fitness after its initialization. Then the 50 children (mutated and non mutated) are replaced with the existing population according

TABLE 2. Switching angles (in radians) corresponding to modulation index m derived from GA.

m	α_1	α_2	α_3	α_4	α_5	α_6
1.1	0.023	0.063	0.100	0.156	0.176	0.239
1.0	0.008	0.068	0.105	0.142	0.191	0.230
0.9	0.027	0.069	0.109	0.167	0.196	0.252
0.8	0.044	0.091	0.154	0.215	0.277	0.335
0.7	0.030	0.092	0.093	0.183	0.215	0.302
0.6	0.037	0.070	0.108	0.142	0.178	0.221
α7						
1.1	0.267	0.318	0.361	0.403	0.449	0.502
1.0	0.272	0.316	0.364	0.402	0.452	0.502
0.9	0.303	0.334	0.412	0.423	0.502	0.536
0.8	0.405	0.4618	0.532	0.610	0.680	0.760
0.7	0.345	0.408	0.471	0.543	0.616	0.683
0.6	0.256	0.297	0.346	0.389	0.434	0.487
α13						
1.1	0.537	0.603	0.637	0.704	0.750	0.814
1.0	0.538	0.607	0.635	0.708	0.749	0.818
0.9	0.602	0.650	0.712	0.771	0.837	0.907
0.8	0.852	0.950	1.069	1.187	1.421	1.571
0.7	0.762	0.829	0.904	1.0100	1.082	1.190
0.6	0.528	0.573	0.629	0.668	0.720	0.773
α19						
1.1	0.873	0.943	1.013	1.105	1.210	1.339
1.0	0.873	0.946	1.015	1.108	1.214	1.345
0.9	0.983	1.074	1.178	1.305	1.563	1.568
0.8	1.571	1.571	1.571	1.571	1.571	1.571
0.7	1.436	1.516	1.520	1.521	1.552	1.565
0.6	0.848	0.914	0.984	1.029	1.131	1.253
α20						
1.1	0.873	0.943	1.013	1.105	1.210	1.339
1.0	0.873	0.946	1.015	1.108	1.214	1.345
0.9	0.983	1.074	1.178	1.305	1.563	1.568
0.8	1.571	1.571	1.571	1.571	1.571	1.571
0.7	1.436	1.516	1.520	1.521	1.552	1.565
0.6	0.848	0.914	0.984	1.029	1.131	1.253
α21						
1.1	0.873	0.943	1.013	1.105	1.210	1.339
1.0	0.873	0.946	1.015	1.108	1.214	1.345
0.9	0.983	1.074	1.178	1.305	1.563	1.568
0.8	1.571	1.571	1.571	1.571	1.571	1.571
0.7	1.436	1.516	1.520	1.521	1.552	1.565
0.6	0.848	0.914	0.984	1.029	1.131	1.253
α22						
1.1	0.873	0.943	1.013	1.105	1.210	1.339
1.0	0.873	0.946	1.015	1.108	1.214	1.345
0.9	0.983	1.074	1.178	1.305	1.563	1.568
0.8	1.571	1.571	1.571	1.571	1.571	1.571
0.7	1.436	1.516	1.520	1.521	1.552	1.565
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0.8	1.571	1.571	1.571	1.571	1.571	1.571
0.7	1.436	1.516	1.520	1.521	1.552	1.565
0.6	0.848	0.914	0.984	1.029	1.131	1.253
α24						
1.1	0.873	0.943	1.013	1.105	1.210	1.339
1.0	0.873	0.946	1.015	1.108	1.214	1.345
0.9	0.983	1.074	1.178	1.305	1.563	1.568
0.8	1.571	1.571	1.571	1.571	1.571	1.571
0.7	1.436	1.516	1.520	1.521	1.552	1.565
0.6	0.848	0.914	0.984	1.029	1.131	1.253

to their fitness. If the fitness of the child is poorer than the already existing solution, this child is discarded. These iterations continue until a pre-decided number is not reached. Here, the number of iterations is set to 5000, which is denoted by K in the flowchart. δ is the current iteration. The angles are generated for 51 values of the modulation index (m), where m is the ratio of the desired fundamental voltage to the maximum achievable voltage. Here, the maximum achievable voltage is 1.714 times the maximum DC voltage applied. The 51 samples of m for which the angles are derived vary from 0.6 to 1.1. The optimum results of all 24 angles corresponding to a few values of m thus generated are shown in Table 2.

V. ANN BASED CONTROLLER

Artificial Neural Networks (ANN) are robust control structures that improvise and improve themselves by imitating human learning behavior. The human learning process is complex and difficult to explain in an affordable mathematical sense. Thus, it is required that the ANN must have a simple structure, and the process learning must also be simple; at least simple to understand. This section discusses a simple neural network based on multi-layer perceptron, in which the learning process is achieved by a back-propagation method which is based on error correction learning.

A. NEURAL NETWORK STRUCTURE

A basic neuron or a single-layer perceptron is shown in Fig. 7(a). The input data (x_1, x_2, \dots, x_n), also known as an

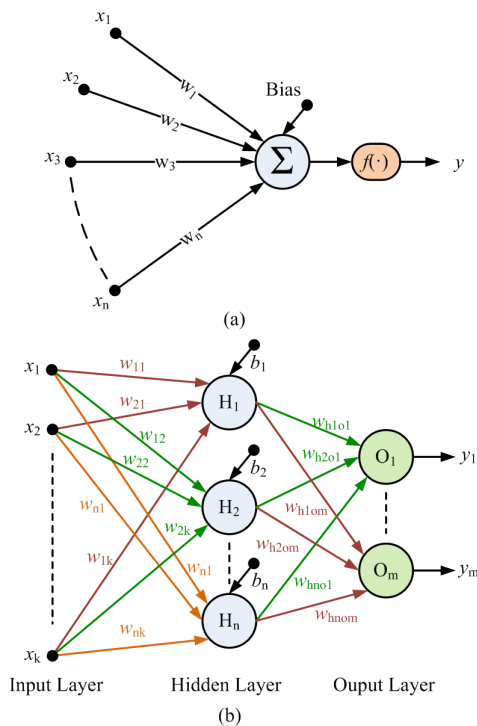


FIGURE 7. Artificial Neural Network: (a) basic neuron, and (b) multi-layer perceptron.

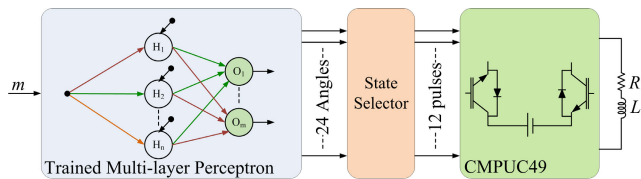


FIGURE 8. Implementation of multi-layer perceptron as a controller for the operation of CMPUC49 with SHM.

epoch, is given to the summer, which behaves as the processor of the unit. The data fed to the nucleus is weighted with the weights defined in such a manner that the output is justified. The output of the processor is given to an activation function which generally is a threshold function. Here it is a binary threshold function. The function introduces the non-linearity in the control structure, which is best suited for power electronic conversion systems for its binary control. Fig 7(b) shows the actual neural network employed for the purpose here. It is a multi-layer perceptron (MLP) structure, and its weights can be determined offline by back-propagation of error or by the Lavenberg-Marquardt (LM) technique. The latter is employed here and discussed in the next subsection. The input to the finally trained ANN will be the voltage level desired and the network must be capable of generating the sought output in terms of 24 angles.

The MLP has multiple layers of neurons, namely, the input layer (which forms the input to the system), the hidden layer, and the output layer. Generally, the number of neurons in the hidden layer is more than the input layer. This is done to increase the dimensionality of the network and make the

data separable. The data which may not be distinguishable in n dimensions, might be separable in $n - 1$ dimensions. This introduces a new problem of training of such networks. This introduces a new problem of training of such networks. Training requires the optimal setting of the weights of the network links. Researchers have done commendable job in offering solutions to such problems, some of which are also discussed in [30].

B. TRAINING OF THE NETWORK

The offline training of the ANN requires a negligible error between the desired result and the one given out by the network. In order to achieve this training, researchers have proposed various techniques based on classical and metaheuristic approaches. In this work a classical LM based technique is employed. The network for this problem has one input and 24 outputs. The hidden layer has 10 neurons. The generalized theory of this technique is discussed as follows. Let us consider a k^{th} neuron of the p^{th} layer that is connected to the n^{th} neuron of the previous layer, and is to be updated. The overall error that has to be minimized for a particular output is given as:

$$e_j = y_j - f(x_i, w_{k,n}^p) \tag{13}$$

where i varies from 1 to k and j varies from 1 to n . The total error that is to be minimized can be expressed as the mean square error of all the errors for N data samples as:

$$E = \frac{1}{N} \sum_{l=1}^N e_j^2 \tag{14}$$

The weight updating algorithm for any weight is given by:

$$\gamma_{k+1} = \gamma_k - \beta_k^{-1} \cdot \delta_k \tag{15}$$

where $\gamma_k = w_{k,n}^p$, and β_k and δ_k are LM parameters which are defined as:

$$\begin{aligned} \beta_k &= \nabla^2 E(\gamma)|_{\gamma=\gamma_k} \\ \delta_k &= \nabla E(\gamma)|_{\gamma=\gamma_k} \\ [\nabla E(\gamma)]_l &= \frac{\partial E(\gamma)}{\partial \gamma_l} \\ &= 2 \sum_{l=1}^N e_j(\gamma) \cdot \frac{\partial e_j(\gamma)}{\partial \gamma_l} \end{aligned} \tag{16}$$

where the gradient $\nabla E(\gamma)$ is rewritten in terms of the Jacobian matrix as:

$$\nabla E(\gamma) = 2J(\gamma) = 2 \begin{bmatrix} \frac{\partial e_{11}}{\partial \gamma_1} & \frac{\partial e_{11}}{\partial \gamma_2} & \dots & \frac{\partial e_{11}}{\partial \gamma_N} \\ \frac{\partial e_{21}}{\partial \gamma_1} & \frac{\partial e_{21}}{\partial \gamma_2} & \dots & \frac{\partial e_{21}}{\partial \gamma_N} \\ \vdots & \vdots & \vdots & \vdots \\ \frac{\partial e_{j1}}{\partial \gamma_1} & \frac{\partial e_{j1}}{\partial \gamma_2} & \dots & \frac{\partial e_{j1}}{\partial \gamma_N} \end{bmatrix}^T \tag{17}$$

The Hessian matrix $\nabla^2 E(\gamma)$ is defined as:

$$[\nabla^2 E(\gamma)]_{k,l} = \frac{\partial E(\gamma)}{\partial \gamma_k \partial \gamma_j} \tag{18}$$

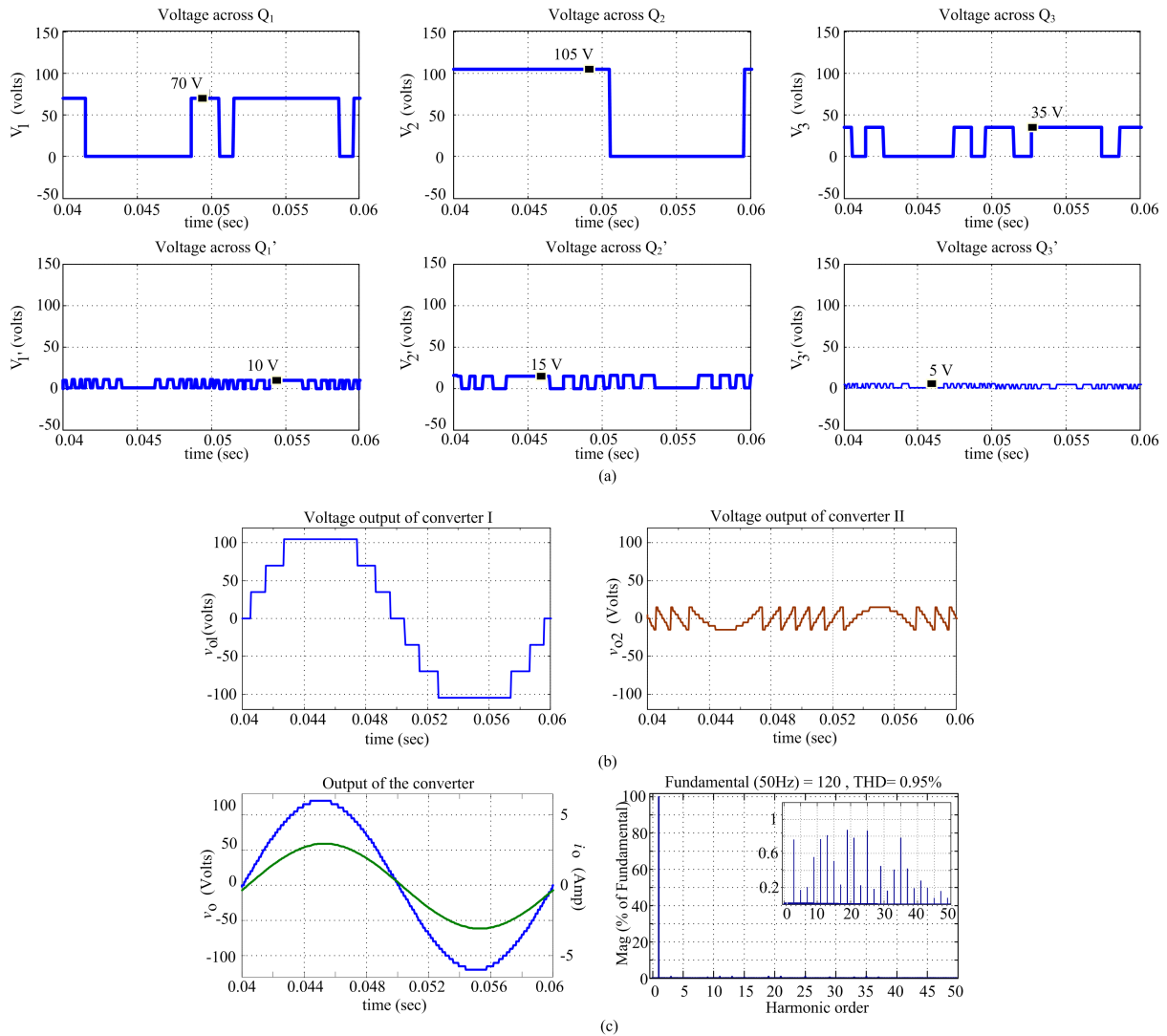


FIGURE 9. Simulation Results: (a) Stress across various switches of CMPUC49, (b) output voltage of each converter, and, (c) load voltage and current of the converter.

which can be further simplified as $2J(\gamma)^T J(\gamma)$, and based on this approximation a simplified expression for γ_{k+1} is given as:

$$\gamma_{k+1} = \gamma_k - [J(\gamma_k)^T J(\gamma_k) + \mu I]^{-1} J^T(\gamma_k) e(\gamma_k) \quad (19)$$

where μ is a variable that changes with every iteration as $\mu_{k+1} = \mu_k \cdot \sigma$ or μ_k / σ , depending on $E(\gamma)_{k+1} \leq E(\gamma)_k$ or $E(\gamma)_{k+1} > E(\gamma)_k$, respectively.

C. IMPLEMENTATION OF THE NETWORK

The implementation of the trained network is shown in Fig. 8. The parameters employed to train the network are chosen as shown in Table 3. It takes a few random iterations before a particular weight of the connection is set. The data for which the network is trained is derived through GA algorithm, whose results are shown in Table 2. The convergence stops as soon as the least mean square error is achieved. Once the network is trained, it is utilized as shown in Fig. 8.

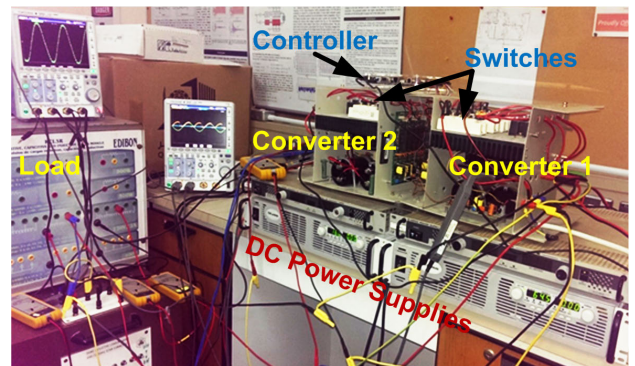


FIGURE 10. Experimental setup of CMPUC49.

VI. RESULTS

The proposed Cascaded MPUC employed with ANN controller is simulated in MATABL/Simulink environment to validate its effectiveness. In this work, the open-loop

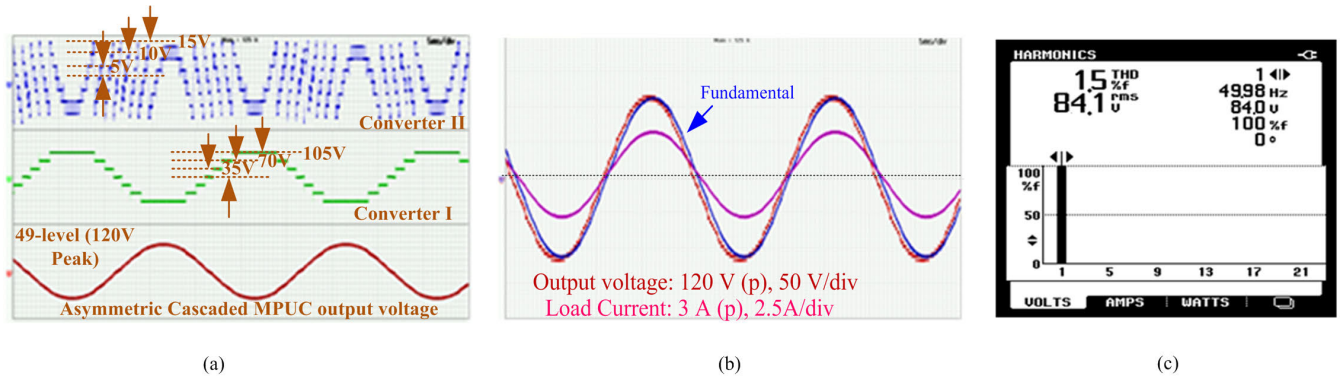


FIGURE 11. Experimental Results: (a) output voltage of each converter, (b) load voltage and current of the converter, and, (c) harmonic spectrum of output voltage.

TABLE 3. Training parameters of ANN.

S. No.	Parameter	Value
1.	Input neurons	01
2.	Hidden layers	01
3.	Hidden neurons	10
4.	Output neurons	24
5.	Iterations	550
6.	Method	LM
7.	μ_0	0.001
8.	σ	0.1

TABLE 4. Parameters of experimental setup.

S. No.	Parameter	Value
1.	DC Sources of converter I	70 V, 35 V
2.	DC Sources of converter II	10 V, 5 V
3.	Load parameters	40 Ω , 10 mH
4.	Controller board	Xilinx Vertex-5

operation of the converter with all voltage sources as DC supplies is considered. The parameters employed for this converter are discussed in Table 4. Figure 9 demonstrates the simulation results. Voltage stress across the switches of the converter shows that the stress is highest on the middle switches (that is across Q_2 in converter 1 and across $Q_{2'}$ in converter 2). Correspondingly, the frequency of switching of these switches is the lowest (at fundamental frequency) with respect to other switches of the respective converter, that is the switching frequency of Q_2 and Q_4 in converter 1 and $Q_{2'}$ and $Q_{4'}$ in converter 2 will lowest of all the switches of the converter. The overall frequency behavior of the switches is as follows: $f_{Q_{3'}} = 2f_{Q_{1'}} = 3f_{Q_{2'}} = 4f_{Q_3} = 5f_{Q_1} = 6f_{Q_2}$, with $f_{Q_2} = 50$ Hz. Also, the voltage stress across these switches vary as follows: $V_{Q_2} = 1.5V_{Q_1} = 3V_{Q_3} = 7V_{Q_{2'}} = 10.5V_{Q_{1'}} = 21V_{Q_{3'}}$, with $f_{Q_2} = 50$. These behaviors can be seen easily observed from Fig. 9(a). The same is true for the complimentary switches (that is $Q_5, Q_4, Q_6, Q_{5'}, Q_{4'}, Q_{6'}$). In Fig 9(b), the individual output of each converter is shown. The output waveform of converter 1 is stepped and has a maximum voltage of 105 V, while the maximum value of the stepped output voltage of converter 2 is 15 V. From these results it can be inferred that the switches of converter 1 must be high-voltage rating low-switching frequency, whereas,

the switches of converter 2 have to block a very small amount of voltage. Thus, GTOs can be employed for converter 1 and IGBTs or MOSFETs for the second. Here, however, for the sake of simplicity, IGBT modules (of two switches) have been employed. The overall converter output of 49 levels is shown in Fig 9(c). The output peak is 120 V, which is 1.714 times the maximum applied voltage, as discussed in (2).

Figure 10 exhibits the experimental setup employed to validate the simulation results and has been obtained by slight modifications in the same prototype that was employed by the authors in [20]. The test rig consists of two MPUC units, DC power sources, RL load and an Xilinx Vertex-5 FPGA controller. Each MPUC unit consists of six switches and is connected to two DC sources. The fin side of the heat sink is cooled by using a fan. The experimental results are shown in Fig. 11. In Fig. 11(a), the output of each converter, that is a 7-level output, is exhibited. The output of converter 1 is a stepped wave of higher voltage rating and corresponds to the first wave of the Fig. 9(b); and the output of the second converter is also a stepped wave of lower voltage rating which corresponds to the second wave of Fig. 9(b). The final wave of Fig. 11(a) is the 49-level output voltage with the output 1.714 times the maximum DC-link voltage applied in the converter. The output voltage, its fundamental component and the load current are shown in Fig. 11(b). The THD of the output waveform is shown in Fig. 11(c), which exhibits 1.5%, and is under the prescribed limit given by IEEE.

VII. CONCLUSION

This paper discusses a boosted output 49-level asymmetrical inverter. A cascaded operation of two 7-level modified PUC inverters (MPUC) with a voltage ratio 1 : 7 between the main DC-links, and 1 : 2 within the sources of individual converters led to such operation. The converter operation with all its switching states and analytics was discussed in detail. In order to minimize the harmonics, switching angles were derived by employing a metaheuristic approach. The technique employed in this work was GA. 24 angles were generated for various output voltage conditions, with modulation

index ranging from 0.6 to 1.1. The ANN was then trained using the LM back propagation technique for all these modulation index-angle combinations. This technique ensures minimum mean square error between the data set results and the practical results. Although, the objective function was set for harmonic elimination, the non-exact behavior of GA and ANN led to retainment of a certain amount, and instead resulted in harmonic mitigation. The converter results were then verified in simulation in MATLAB/Simulink[®], which were further validated on an experimental setup. The harmonic content of the voltage obtained was within the prescribed limit of IEEE.

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