Off – Grid Power Supply Solution for Portable Cabins using Solar PV System for Qatar

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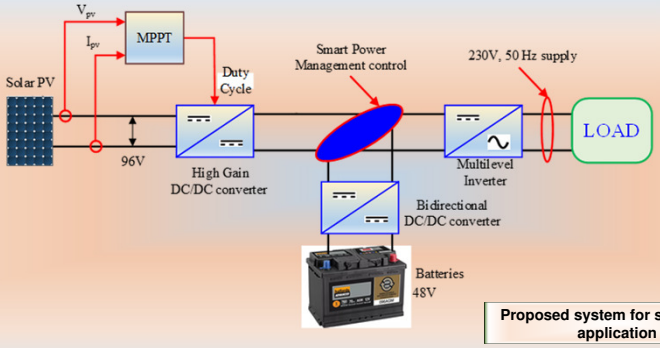
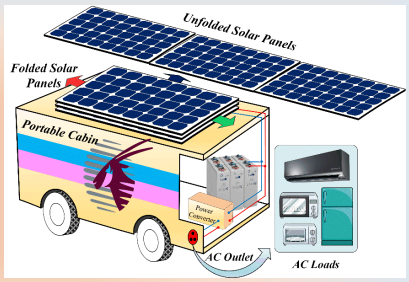
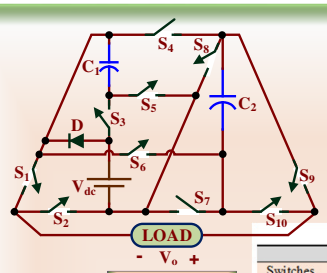
In this project, a new system for power supply for remote area has been proposed. In the proposed system, solar PV based system with battery storage for stand-along application has been discussed. The use of multilevel inverter and high-gain DC/DC converter has been proposed in this system. The proposed multilevel inverter generates nine-level output voltage waveform with quadruple voltage gain. The proposed DC/DC converter is based on the concept of switched-inductor with voltage lift switched-capacitor and has been verified for a voltage gain of 20. The experimental results confirmations the satisfactory performance for stand-alone applications of the proposed converters.





Proposed system for standalone application

Proposed Quadruple Multilevel Inverter

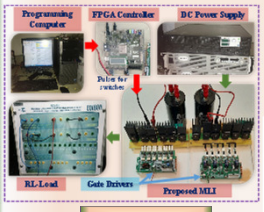


Proposed Topology

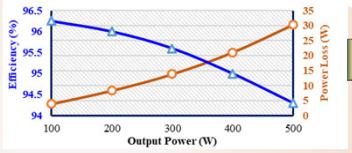
- Single source configuration
- Requires only two capacitors for a voltage gain of 4
- 10 switches and one diode is used
- Both capacitors are self-balanced
- Voltage stress of individual devices is lower than the peak output voltage

EXPERIMENTAL PROTOTYPE DETAILS

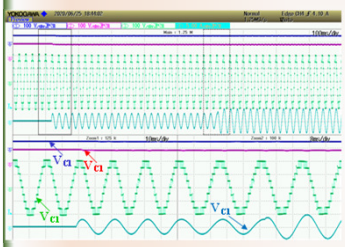
Key Components	
Switches	G60N100 IGBT
Capacitor	PG6DI (450V and 2200μF)
Controller	FPGA Vertix-5 (XC5VLX50T)
Gate Driver	GDA-2A4S1
dc power supply	TDK Lambda GEN300-11
Key Parameters	
Resistive + Inductive loads	Two sets of 80Ω-80mH
Input dc Link Voltage	50V
Output Voltage	200V (peak)
Fundamental/Switching Frequency	50Hz/5kHz



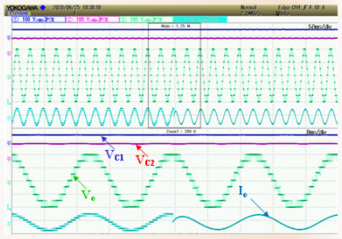
Experimental setup



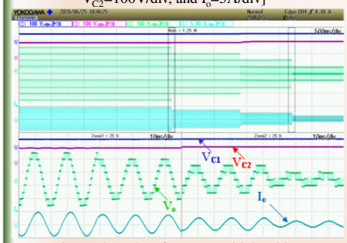
Efficiency Plot



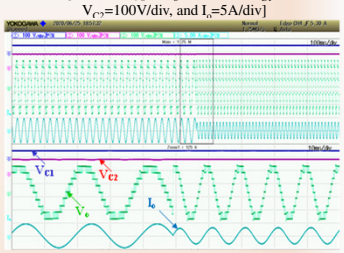
Experimental results of a proposed 9-level inverter with change in RL load [V_o=100V/div, V_{C1}=100V/div, V_{C2}=100V/div, and I_o=5A/div]



Experimental results of a proposed 9-level inverter with change in load type [V_o=100V/div, V_{C1}=100V/div, V_{C2}=100V/div, and I_o=5A/div]



Experimental results of a proposed 9-level inverter with a step change in MI.



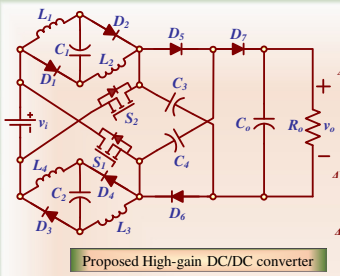
Experimental results of a proposed 9-level inverter with change in output frequency.

COMPARISON TABLE FOR DIFFERENT 9 LEVEL TOPOLOGIES WITH QUADRUPLE VOLTAGE GAIN

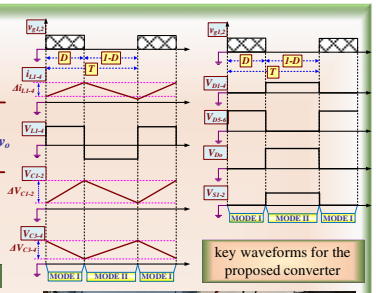
Top	N_{sw}	N_{gd}	N_d	N_{com}	N_c	VRC V_{dc}	VRC $2V_{dc}$	N_{dc}	TSV_{pu}	TCD $\pm1^{st}$	TCD $\pm2^{nd}$	TCD $\pm3^{rd}$	TCD $\pm4^{th}$	TCD_{avg}	CF (with value of α and β) 0.5, 0.5	1.0, 1.0	1.5, 0.5	0.5, 1.5
[1]	17	17	0	17	3	3	0	9	5.5	8	8	8	8	8	35.75	42.5	41.25	43.75
[2]	8	8	3	11	3	1	2	6	5.75	5	5	5	5	5	27.375	32.75	33.125	32.375
[3]	12	12	0	12	2	1	1	6	5.25	6	7	7	6	6.5	26.875	32.75	32.125	33.375
[4]	17	17	5	22	4	4	0	12	5.5	10	9.5	8	8.5	9	45.25	52.5	50.75	54.25
[5]	13	13	0	13	3	3	0	6	6.25	8	7	6	5	6.5	28.375	34.75	34.625	34.875
[6]	8	8	6	14	3	3	0	6	8	8	4	5	5	5.5	29.75	36.5	37.75	35.25
[7]	10	10	3	13	3	3	0	6	6.25	8	5	5	5	5.75	28	34	34.25	33.75
[P]	**10**	**10**	**1**	**11**	**2**	**1**	**1**	**4**	**5.75**	**5**	**5**	**5**	**4**	**4.75**	**23.25**	**28.5**	**29**	**28**

$N_{sw}/N_{gd}/N_d/N_{com}/N_c$/VRC = Number of switches/number of gate driver circuit/number of diodes/total number of components ($N_{sw}+N_d$)/number of capacitor/voltage rating of capacitors, N_{dc} = Number of devices in charging loop, TSV_{pu}=Total standing voltage in per unit, TCD = Total conducting device,

Proposed High-gain DC/DC converter



Proposed High-gain DC/DC converter

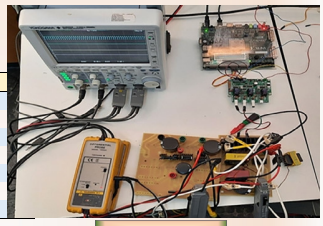


key waveforms for the proposed converter

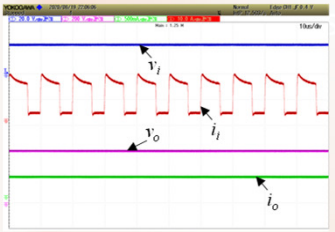
Voltage Gain $\frac{V_o}{V_{in}} = \frac{7+D}{1-D}$

Experimental Parameters

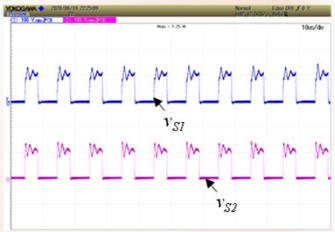
Parameter	Value
Input voltage	22V
Switching frequency	50kHz
Inductor (L_1 and L_2)	1mH
Capacitors (C_1 and C_2)	220μF
Capacitor C_o	470μF
Controller	FPGA Vertix-5 (XC5VLX50T)
Load Resistance	400Ω-800Ω



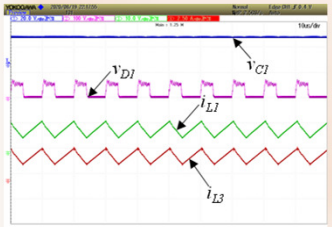
Experimental setup



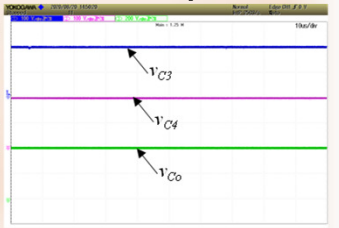
Experimental results of input and output voltage and current



Experimental results of voltage stress of switches S_1 and S_2



Experimental results of voltage of capacitor C_1, diode D_1 and inductor current of i_{L1} and i_{L3}



Experimental results of voltage of capacitor C_3, C_4 and C_o.

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[6] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014.
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