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A New Eight Switch Seven Level Boost Active Neutral Point Clamped (8S-7L-BANPC) Inverter

ATIF IQBAL[1], (Senior Member, IEEE), MARIF DAULA SIDDIQUE[1], (Member, IEEE), JAGABAR SATHIK MOHAMED ALI[2], (Senior Member, IEEE), SAAD MEKHILEF[3,4], (Senior Member, IEEE), AND JOHN LAM[5], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Qatar University, Doha, Qatar
[2]Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai 603203, India
[3]Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
[4]School of Software and Electrical Engineering, Swinburne University of Technology, Melbourne, VIC 3122, Australia
[5]Department of Electrical Engineering and Computer Science, York University, Toronto, ON M3J 1P3, Canada

Corresponding author: Marif Daula Siddique (marif.daula@qu.edu.qa)

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ABSTRACT A new boost Active-Neutral-Clamped (ANPC) voltage boosting inverters are appealing for low dc-link voltage demand. Recent boost ANPC topology has demonstrated a 1.5 times voltage gain, but the number of switches has a higher number. This paper proposed an improved boost ANPC topology with 1.5 voltage gain using the least number of switches. Further, the number of conducting switches has been reduced remarkably which enhances the system efficiency. The seven-level (7L) output voltage levels are achieved using a floating capacitor with self-voltage balancing capability. The proposed topology has been analyzed and compared to the ANPC topologies proposed in recent years. For the validation of the theoretical aspect of the proposed topology, the experimental findings have been compiled in the paper.

INDEX TERMS Multilevel inverter (MLI), active neutral point clamping (ANPC) inverter, seven-level (7L), boost inverter, reduced switch count.

I. INTRODUCTION

In recent times, Multilevel Inverters (MLIs) have been focused on small, medium, and high power applications and have been investigated extensively. The rapid growth and demand of MLIs in energy, utilities, high-frequency power, and renewable power generation has been a key element. Low voltage stress, improved efficiency, and high modularity are some of the benefits of the MLIs. The classic single-dc MLI structures like flying capacitor MLI and diode clamped MLI have voltage balance constraints. In comparison, cascaded H-bridge (CBH) MLI is highly modular and reliable, however, many isolated dc sources are necessary. To decrease the dc source count for a higher number of levels, the CHB-MLI was restructured with the asymmetrically configured sources [1]–[3].

With a conventional system, the required load voltage can be achieved by taking into consideration of multiple PV panels, dc-dc converters, and a transformer. The total size of the system and overall losses are therefore increasing. Multilevel inverters are preferred for applications with photovoltaic (PV) or fuel-cell systems due to the reduced voltage stress of switches that leads to lower losses with reduced cost. The neutral point based multilevel inverters are becoming popular as the solid connections between the dc link and the grid through the neutral point with a neutral point clamping (NPC) or active neutral point clamping (ANPC) topologies hold the common voltage constant at a very low value, which reduces the leakage current in the systems. This feature appeals equally to the motor drives and marine power supply [4], [5].

Fig. 1 categorizes the different types of MLI topologies. Huge research has been done on the establishment of ANPC inverters of higher levels, but at the expense of the voltage-balance issue. Further voltage-balancing circuits are usually needed to solve the balance problem, with specially designed control algorithms [6], [7]. With the applications related to the solar PV systems, the boosting of the input voltage

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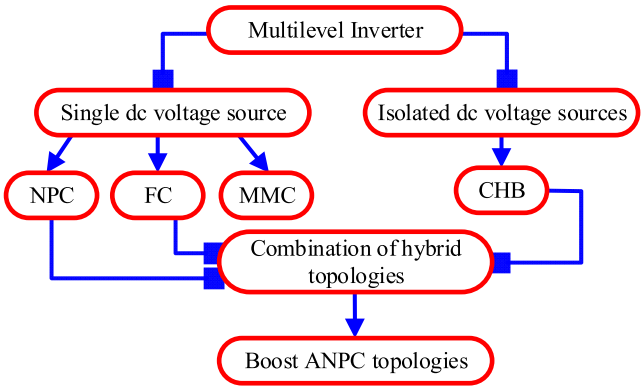

FIGURE 1. Classification of multilevel inverter topologies.

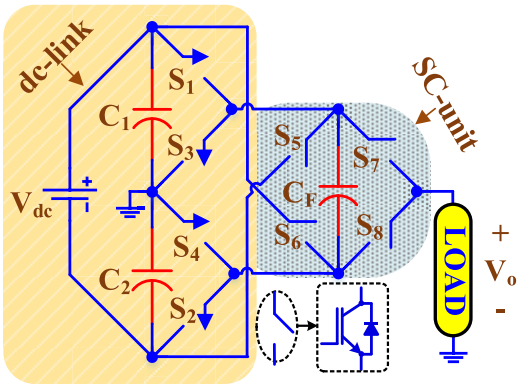

FIGURE 2. Proposed 8S-7L-BANPC inverter topology.

is necessary for high voltage applications. The switched-capacitor (SC) principle has been used as a research phenomenon to boost the input voltage with multi-stepped output voltages. In SC-based topologies, the switched capacitors are connected in parallel to the input voltage source for charging purposes and then in series to achieve a high voltage output [8]–[10]. More recently, the researchers investigated a new form of single-stage boost inverter based on ANPC for the solar PV system due to the availability of the neutral point. Some studies have tried to develop ANPC inverters with reduced switch count, thereby improving performance. The author in [11] attempted by adequately incorporating a floating capacitor to increase the voltage gain of the traditional 3L ANPC from half to unity with 5L output. Another topology suggested by [12], uses similar principles of the floating capacitor to enhance the boosting level. The voltage gain was increased to 1.5, however, two floating capacitors with a voltage rating equal to the input voltage increases the overall cost of the inverter. Further improvement to the boost inverter topology has been suggested in [13]–[22]. However, one major concern has been the number of conducting switches along with the number of switches in the charging path of the floating capacitor. As the charging current has a higher magnitude for a small duration, the current rating of the switches in the charging path must be of higher value which increases the cost and losses. In the above topologies, the number of conducting switches is on the higher side along with the overall number of switches. Therefore, the cost and power losses are on the higher side.

In this paper, an improved boost ANPC inverter topology has been proposed which overcomes the issue of a higher number of devices in the conducting and charging path. The proposed topology uses eight switches with a single floating capacitor to achieve 7L output voltage with a voltage gain of 1.5. The remaining paper is structured as follows: the operation of the proposed topology along with power loss analysis is discussed in Section II, followed by a comparative study in Section III. The experimental results are discussed in section IV, and finally, the paper has been concluded in section V.

TABLE 1. Voltage stress ($\times V_{dc}$) of different switches.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
1	1	1.5	0.5	2	0	0	1	$1.5V_{dc}$
0.5	0.5	1	0	1.5	0.5	0	1	V_{dc}
0	0	0.5	0.5	1	1	0	1	$0.5V_{dc}$
0.5	0.5	0	1	0.5	1.5	0	1	Zero
0.5	0.5	1	0	1.5	0.5	1	0	
0	0	0.5	0.5	1	1	1	0	$-0.5V_{dc}$
0.5	0.5	0	1	0.5	1.5	1	0	$-V_{dc}$
1	1	0.5	1.5	0	2	1	0	$-1.5V_{dc}$

II. PROPOSED 8S-7L-BANPC TOPOLOGY

A. DESCRIPTION OF 8S-7L-BANPC TOPOLOGY

The circuit diagram of the suggested 8S-7L-BANPC topology is shown in Fig. 2. It consists of eight switches, two dc-link capacitors C_1 and C_2, and one floating capacitor C_F. Out of eight switches, four switches, i.e., $S_1 - S_4$ are configured as reverse blocking (RB) i.e., IGBT with a series diodes, which enables the unidirectional current flow. They can also be configured as bidirectional switches for inductive load (a unidirectional switch with 4 diodes). The remaining four switches are IGBTs with antiparallel diodes which enable the bidirectional current flow. Fig. 3 summarizes the switching combinations of the proposed 8S-7L-BANPC topology. One of the main features of the proposed topology has been a lower number of ON states switches for all 7L. During zero, $\pm V_{dc}$, and $\pm 1.5V_{dc}$, only two switches are in ON state and during the voltage levels of $\pm 0.5V_{dc}$, three switches are in ON states. The reduction in the number of ON state switches reduces the conduction losses and thus improves the efficiency of the topology. Further, the floating capacitor is charged during the voltage states of $\pm 0.5V_{dc}$, only two switches, i.e., S_1 and S_2 need to carry the capacitor charging current I_c, which also improves the efficiency. For the proposed topology, the voltage and current stress of each switch are analyzed and summarized in Table 1 and Table 2, respectively.

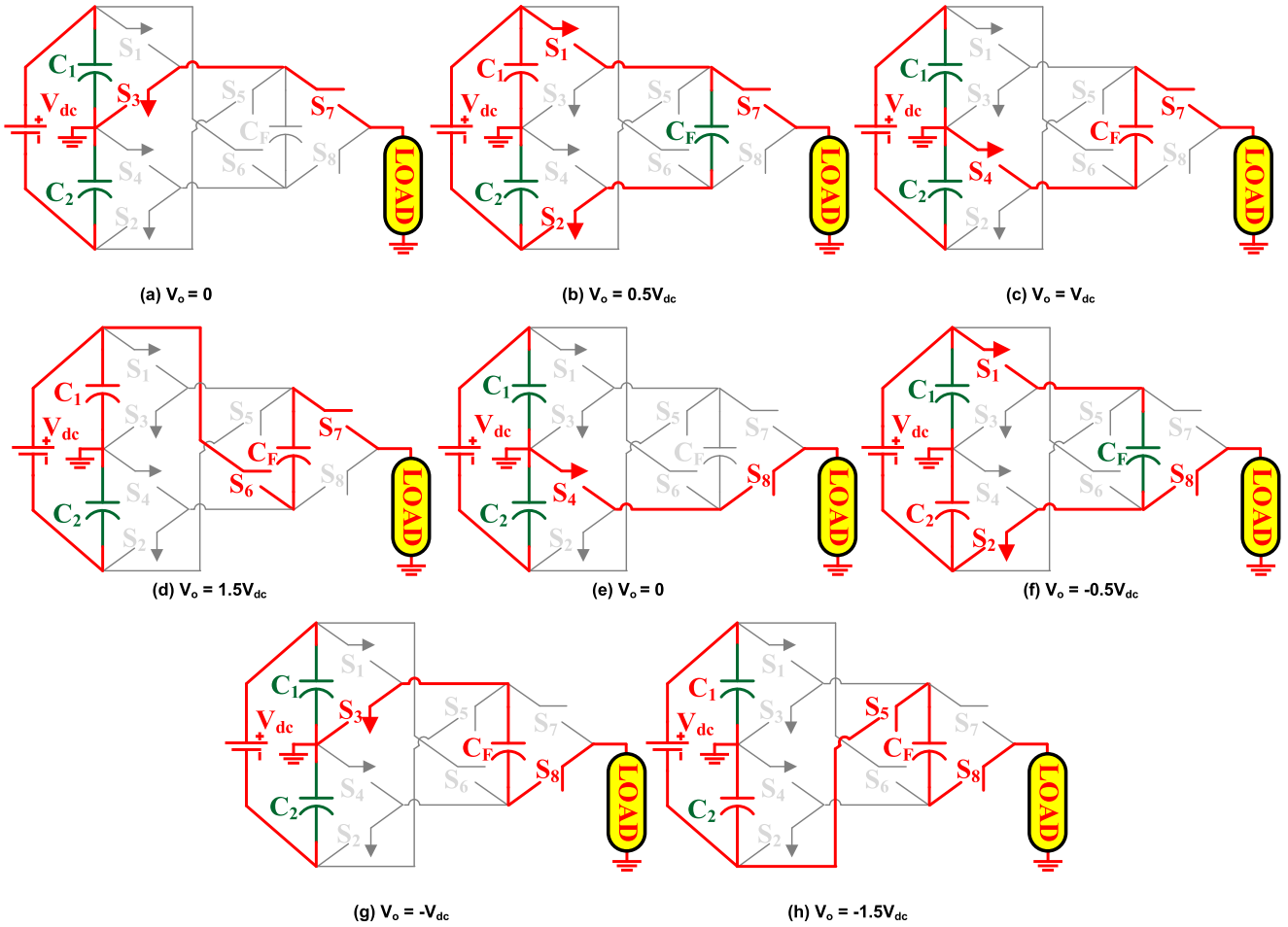

FIGURE 3. Switching states of the proposed topology.

TABLE 2. Current stress of different switches topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
0	0	0	0	0	I_o	I_o	0	$1.5V_{dc}$
0	0	0	I_o	0	0	I_o	0	V_{dc}
I_o+I_c	I_o+I_c	0	0	0	0	I_o	0	$0.5V_{dc}$
0	0	I_o	0	0	0	I_o	0	Zero
0	0	0	I_o	0	0	0	I_o	
I_o+I_c	I_o+I_c	0	0	0	0	0	I_o	$-0.5V_{dc}$
0	0	I_o	0	0	0	0	I_o	$-V_{dc}$
0	0	0	0	I_o	0	0	I_o	$-1.5V_{dc}$

B. CAPACITANCE SELECTION

In switched-capacitor based MLI topologies, the selection of the capacitance value of each capacitor plays an important role. The ripple voltage of the capacitors is the main factor that decides the value of dc-link capacitors C_1 and C_2. As the load current is equally shared by both dc-link capacitors due to the direct connection of the neutral terminal, their ripple voltage can be estimated as

$$\Delta V_{C1} = \Delta V_{C2} = \frac{I_{o,\max}}{X_C} \tag{1}$$

where $I_{o,max}$ is the peak value of load current and X_C is the capacitive reactance offered by the dc-link capacitors.

In the proposed 7L-ANPC topology, the floating capacitor is charged and discharged during the different voltage levels and is charged up to the voltage equal to the input voltage, i.e., V_{dc}. In the MLI topology, the ratings of the floating capacitor depend mainly on the allowable ripple voltage, i.e. ΔV_{CF}. If a continuous line takes over the carrier signals, the output voltage along with the capacitor voltages is illustrated in Fig. 4. As shown in Fig. 4, the floating capacitor C_F has a maximum discharge time (MDT) from t_2 to t_2'. During this time interval, the reduction in the discharge value is calculated as:

$$Q_{CF} = 2\int_{t_2}^{t_2'} I_o\,(\omega t)\,d\,(\omega t) \tag{2}$$

With ΔV_{CF} as the allowable voltage ripple of the capacitor C_F, the optimal value of capacitor C_F is given as

$$C_F = \frac{Q_{CF}}{\Delta V_{CF}} \tag{3}$$

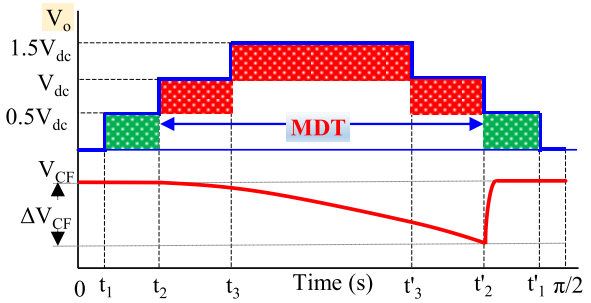

FIGURE 4. Capacitor voltage variation in the worst condition.

C. MODULATION STRATEGY

For the control of the switches of the MLI, the pulse width modulation (PWM) technique is necessary. For this purpose, several PWM techniques have been proposed and are categorized as low switching frequency and high switching frequency modulation technique. Nearest level control (NLC) and selective harmonic elimination (SHE) are the famous PWM technique with low switching frequency [23]–[25]. Multiple carrier PWM, space vector PWM are some of the high switching frequency modulation techniques. Generally, low switching frequency techniques are used for a higher number of levels and high switching frequency modulation techniques are used for a lower number of levels due to better harmonic performance. For the proposed 7L-8S-ANPC inverter, high-frequency PWM technique, i.e., level-shifted PWM (LS-PWM) is used for the generation of the gate pulses for different switches. Six carrier signals (of V_a magnitude each) are compared with the reference sinusoidal signal (V_{sine}) as shown in Fig. 5 (a). The gate pulses and the resultant output voltage has been depicted in Fig. 5 (b) and (c) respectively.

D. POWER LOSS ANALYSIS

The switching and conduction losses are the main losses associated with the power semiconductor devices. Similarly, the ripple losses of the capacitors are the other major losses with the switched capacitor based MLI topology. PLECS software has been used to estimate the losses of an inverter using thermal modeling. The lookup tables are used for the calculation of switching and conduction losses of the devices. The lookup table is made using the various data provided by the manufacturer in the datasheet of the device. Fig. 6 (a) illustrated the variation of the efficiency at different output power. The maximum efficiency of the proposed 8S-7L-BANPC is 97.3%. Further, Fig. 6 (b) shows the power loss distribution among different switches and capacitors. As can be seen from Fig. 6 (b), the power losses of the switches in the charging loop, i.e., S_1 and S_2 have a higher percentage to the overall losses. This is due to the higher charging current of the floating capacitor C_F.

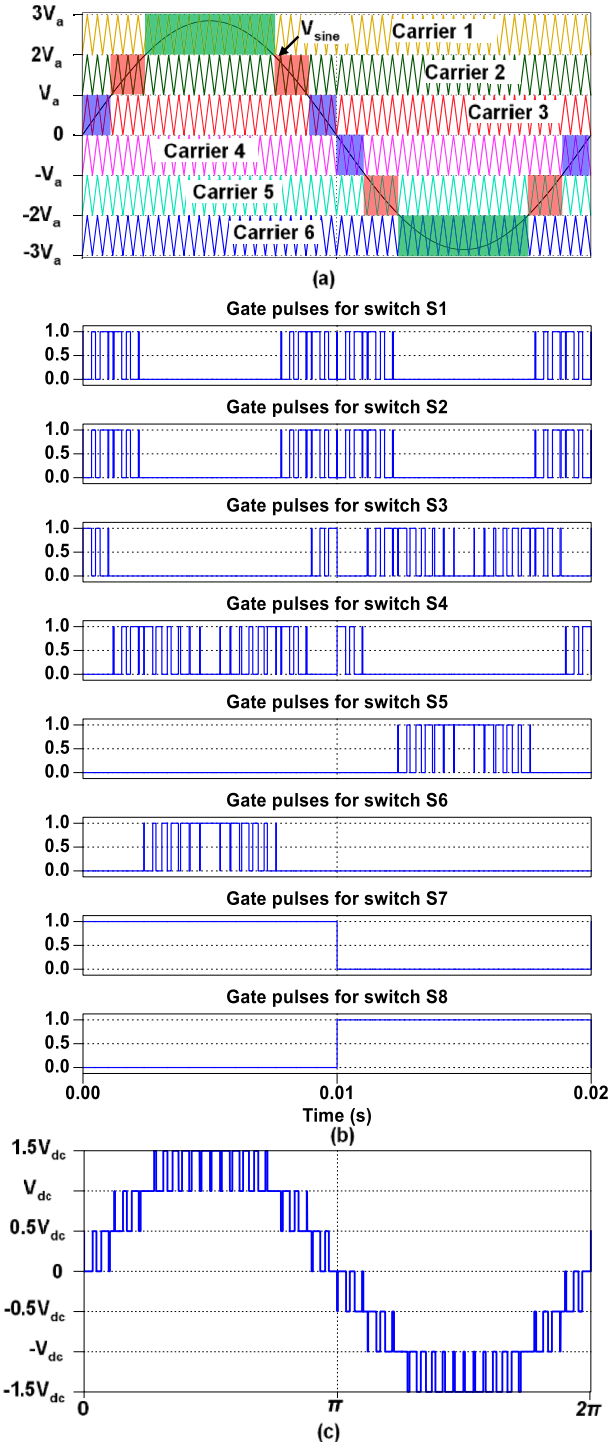

FIGURE 5. Level shifted PWM technique for 7L.

III. COMPARATIVE ASSESSMENT

Table 3 provides comparative assessments between the different 7L MLIs with a single input. For a fair comparison, only topologies with a voltage gain of 1.5 have been considered. From Table 3, only eight switches are used for the proposed

TABLE 3. Comparison between proposed 8S-7L-BANPC and topologies with single source, 1.5 voltage gain configuration.

Top	N_{sw}	N_{gd}	N_c	N_{sc}	$TSV_{p.u.}$	TCS				CF (value of α and β)			
						$\pm 0.5V_{dc}$	$\pm V_{dc}$	$\pm 1.5\ V_{dc}$	TCS_T	0.5, 0.5	1.0, 1.0	1.5, 0.5	0.5, 1.5
[10]	10	8	3	4	5.3	3	3	3	9	27.15	33.3	36.45	30.15
[12]	10	8	4	4	7.3	5	4	5	14	28.98	36.97	40.28	33.65
[13]	9	8	3	4	5.3	6	5	5	16	26.50	33.00	35.17	30.84
[14]	9	8	3	4	5.3	5	4	4	13	27.32	34.63	36.62	32.65
[15]	10	9	3	4	6	5	4	5	14	26.82	33.63	36.12	31.15
[16]	9	8	3	4	5.3	5	5	4	14	29.33	36.67	39.33	34
[17]	9	8	3	3	5.67	5	4	4	13	26.98	33.97	36.28	31.65
[P]	8	8	3	2	7.3	3	2	2	7	24.82	30.63	34.12	27.15

N_{sw}/ N_{gd}/ N_c/ N_{sc} = Number of switches/gate driver/capacitor/switches in charging loop, TSV_{pu}=Total standing voltage (in per unit)

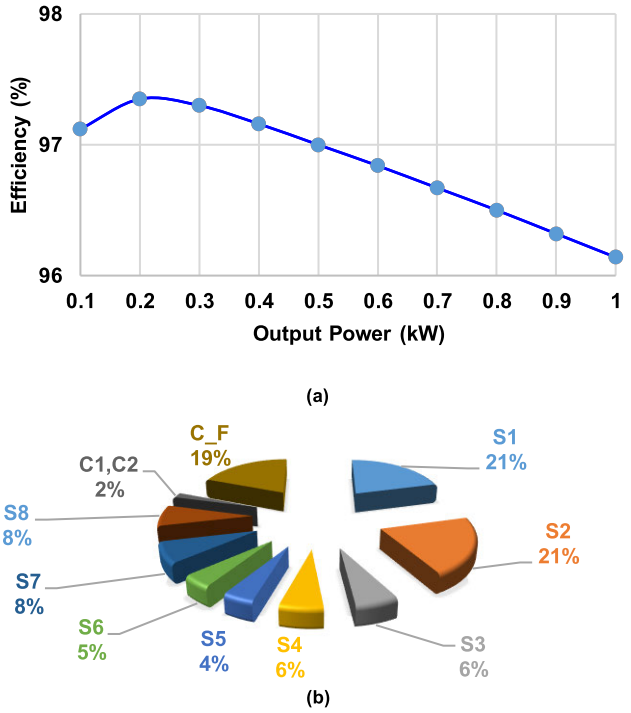

FIGURE 6. Power loss analysis with (a) efficiency curve, (b) power loss distribution.

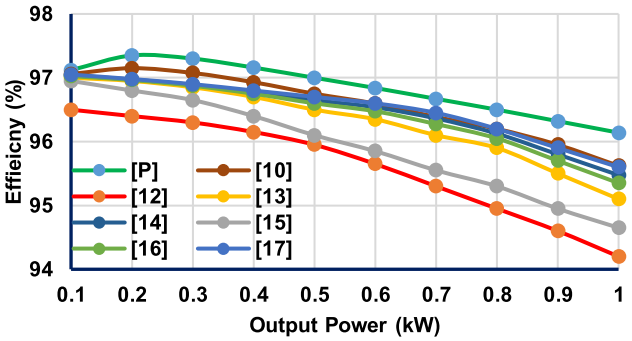

FIGURE 7. Efficiency comparison.

TABLE 4. Simulation and experimental parameters.

Parameter	Simulation	Experimental
Input Voltage	100V, 120V	100V
Capacitors	4700μF	4700μF, 450V
Output frequency	50 Hz	50 Hz
Carrier frequency	5 kHz	5 kHz
Controller	MATLAB	FPGA Virtex-5
Resistive Load	50Ω	30Ω, 15Ω
Inductive Load	100mH	50mH

topology, which is the least among the 7L topologies listed in Table 3. Further, except for the topology proposed in [12], all other topologies including the proposed one require only one floating capacitor.

The number of switches in the charging path has major concern based on switched-capacitor boost MLIs. Due to the design of the proposed topology, only two switches are present in the charging loop of the floating capacitor whereas three switches are required in [17] and four switches in all other topologies. The lower number of switches in the charging path reduces the requirement of the current rating switches.

Another design aspect of the proposed topology has been the number of conducting switches. The switching loss is low because of the lower switching frequency and the voltage stress of the switches of the multilevel inverter. With proper

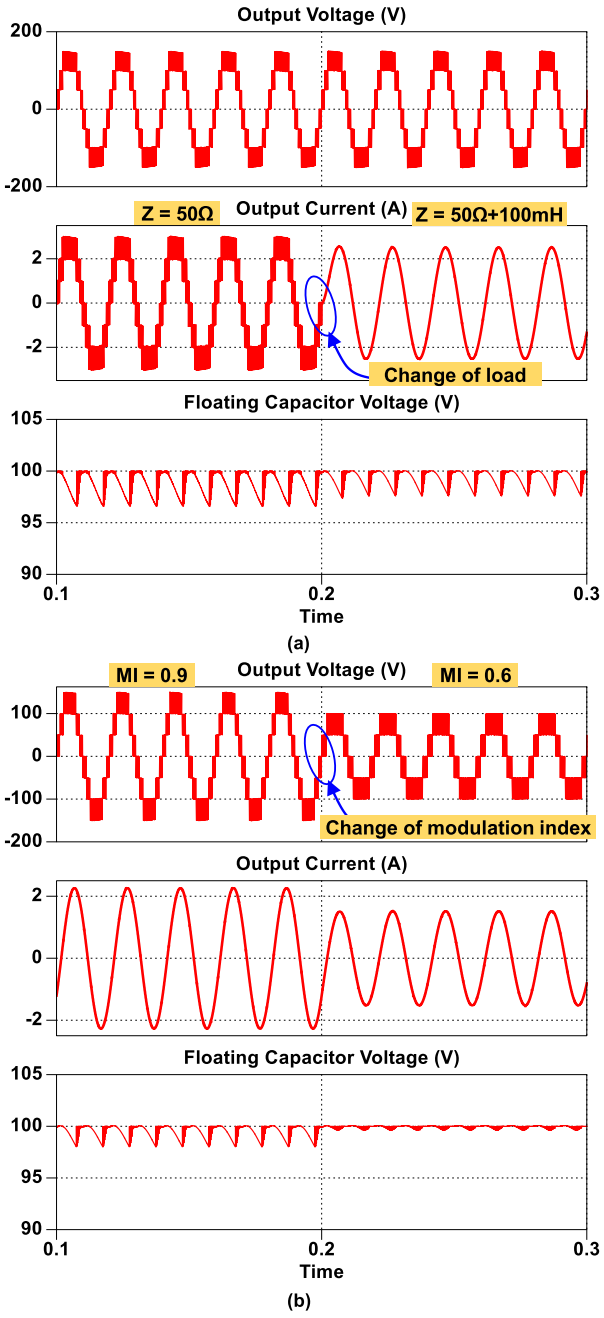

FIGURE 8. Simulation results of the proposed topology with (a) change of load and (b) change of modulation index.

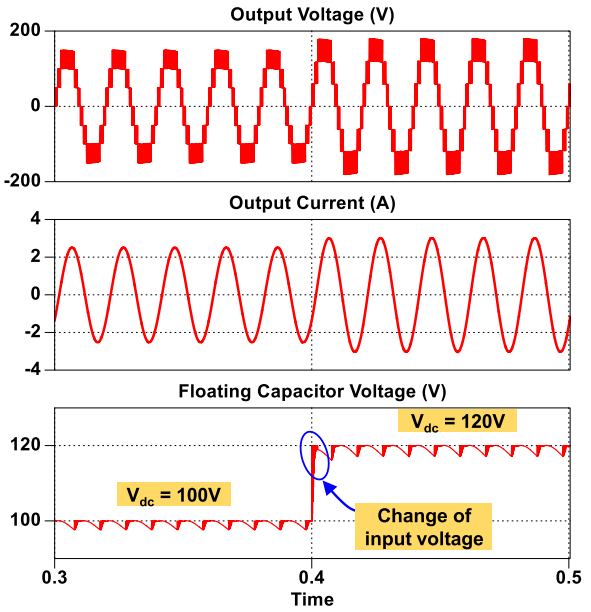

FIGURE 9. Simulation results with change of input voltage.

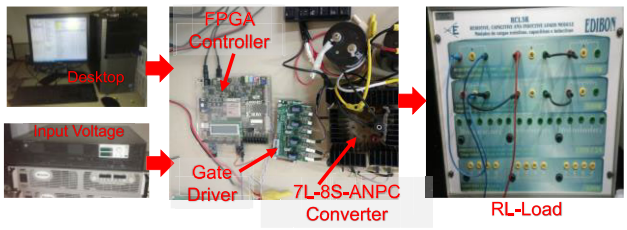

FIGURE 10. Experimental setup.

capacitance calculation, the ripple loss can also be reduced. Therefore, the majority of MLIs losses are due to the conducting losses of the switches. The 7L inverter has three output levels in each half-cycle that are indicated in 1st, 2nd, and 3rd considering the symmetry of output. Table 3 summarized the number of Total Conducting Switches (TCS) in the load current path at each output level. More conduction device leads to a higher loss of power. The TCS is the lowest compared to other topologies at each level of the proposed topology. For the proposed topology, the TCS is only 7, which is 22% less than topology of [10], 43% to [14], [17], 50% to [12], [16], and 64% to the topology suggested in [13].

The cost function (CF) for estimating the total cost of boosting MLI is adopted to further analyze the. The CF value of the topology can be calculated as [26]:

$$CF = N_{sw} + N_{gd} + N_C + \alpha TSV + \beta TCS_{avg} \quad (4)$$

TCS_{avg} is the average value of TCS which is equal to 1/3 of the total TCS, TCS_T. The weight calculation coefficients of TSV and TCS_{avg} are represented by α and β, respectively. In general, if α is selected greater than 1, this means that the voltage stress value is more important than the design part count. Conversely, if α is set below 1, the component's voltage stress is the secondary factor relative to the component count. A similar condition applies to the value of β. The number of dc voltage and voltage gain has not been considered for the calculation of CF as all topologies are the single source with a voltage gain of 1.5. Table 3 gives the calculated CF for different values of α and β. The CF of the proposed 8S-7L-BANPC topology has a lower value compared to all other topologies irrespective of the value of α and β.

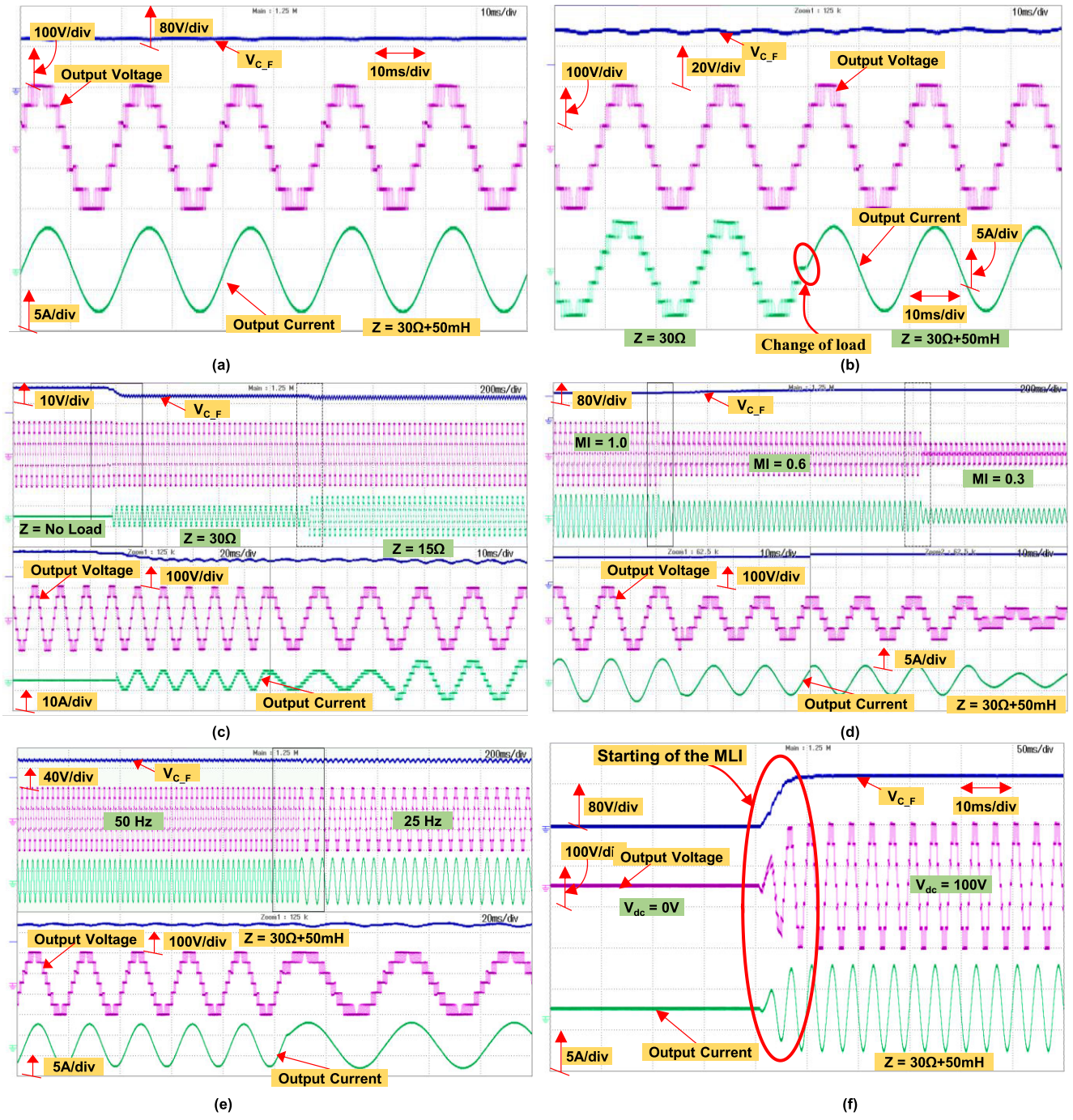

FIGURE 11. Experimental results of the proposed 7L-8S-ANPC topology with (a) RL load, (b) change of load power factor, (c) step change in load, (d) change of modulation index, (e) change of output voltage frequency and (f) starting condition.

Fig. 7 shows an efficiency comparison of different 7L topologies. As depicted in Fig. 7, the efficiency of the proposed topology is better than other topologies. The higher efficiency is due to the lower number of components with lower number of ON-state components. Therefore, all these comprehensive comparisons describe the merit of the proposed topology compares to all other similar topologies.

IV. RESULTS AND DISCUSSION

The theoretical aspect of the proposed 8S-7L inverter has been verified using simulation results considering several operating conditions. Table 4 gives the different simulation and experimental parameters. With the input dc voltage selected as 100V, the dc-link voltage split it into 50V and the floating capacitor is charged up to 100V, i.e., equal to the

input voltage. Fig. 8 (a) shows the output waveforms of voltage, current, and floating capacitor voltage with the change of load. The load is changed from 50Ω to 50Ω+100mH. The change of load occurs at t=0.2s and this change is reflected as the change of nature of the waveform of load current. The peak output voltage is 150V and it shows the voltage gain of 1.5 times the input voltage. Furthermore, the modulation index (MI) of the PD-PWM is changed from 0.9 to 0.6 and the corresponding waveforms are illustrated in Fig. 8 (b) with a load of 50Ω + 100mH. With the reduction in the change of modulation index, the number of levels is reduced. With this case, the number of levels reduces from 7 to 5 as the modulation index is changed from 0.9 to 0.6.

In addition to the above two cases, the proposed topology has been tested with the change of input voltage. Fig. 9 illustrated the change of input voltage from 100V to 120V. All the voltages increase accordingly, i.e., peak output voltage reaches to 180V with the voltage of floating capacitor voltage changes from 100V to 120V at the time instant of t=0.4s. All these simulation results show the self-balancing of the floating capacitor voltage.

To demonstrate the working of the proposed 8S-7L-BANPC topology, a laboratory prototype as shown in Fig. 10, has been used with an input voltage of 100V. The floating capacitor has been selected as 4700μF with the part number of PG6DI. G60N100 IGBT switches have been used to realize the proposed 8S-7L-BANPC topology. The LS-PWM technique with a carrier frequency of 5 kHz has been used for the generation of the gate pulses using the FPGA Spartan 6 (XC5VLX50T) controller. Fig. 11 (a) shows the waveform of output voltage (V_o), current (i_o), and capacitor voltage (V_{C_F}) with a series-connected inductive-resistive load of 50mH and 30Ω. With the input voltage of 100V, the peak of the output voltage with 7L has a magnitude of 150V having a step voltage of 50V, which confirms the voltage gain of 1.5. The floating capacitor voltage is settled at 100V.

Furthermore, the dynamic response of the proposed topology has been tested with dynamic starting and loading conditions. Fig. 11 (b) illustrates the waveforms with a change of load power factor as an R load of 50Ω is changed to an RL load of 30Ω + 50mH. The floating capacitor voltage is balanced with a slight change of its ripple voltage. Furthermore, a step change of load has also been tested with the proposed topology and the corresponding waveforms are depicted in Fig. 11 (c). Initially, the converter operates at the no-load condition and the load current is zero. After that, the load current is changed to 30Ω and then after from 30Ω to 15Ω. The reaction of load resistance by half-value increases the load current by double fold. As the converter is loaded, the floating capacitor voltage shows the drop in the voltage, however a sufficient value of capacitance is used, the drop is limited to less than 10%. Besides, the change of modulation index has been depicted in Fig. 11 (d) with modulation index changes from 1.0 to 0.6 to 0.3. With this change of MI, the number of levels reduces with the reduction of the peak of the load current.

Fig. 11 (e) shows the effect of the variation of the output frequency on the output waveforms. The change of frequency is important for electric motor drive applications. The output voltage frequency is changed from 50Hz to 25Hz. However, this change in frequency has no effect on the balancing of the floating capacitor voltage and it remains balanced irrespective of the output voltage frequency. Furthermore, the starting condition of the proposed topology is shown in Fig. 11 (f). As the input voltage is changed from zero to 100V, the floating capacitor voltage attends 100V magnitude which is equal to the input voltage. The change from 0V to 100V occurs in a few cycles of the output voltage. Fig 11 (f) also shows that the floating capacitor does not require to be pre-charged.

V. CONCLUSION

This paper proposes a new hybrid ANPC inverter with 8 power switches and a floating capacitor. It increased the voltage gain to 1.5 with a 7L output voltage. In addition, it addresses the drawback of the recent topology of having a higher number of conducting switches, which improves efficiency. The proposed 8S-7L-BANPC inverter had been evaluated in depth through various comparison parameters. The feasibility and efficiency of the proposed topology have been validated as an alternative to improve an ANPC inverter by an excellent agreement between theoretical analysis and experimental results.

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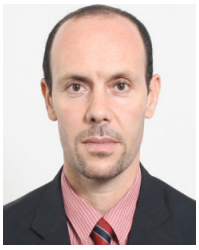
ATIF IQBAL (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in power system and drives (engineering) from Aligarh Muslim University (AMU), Aligarh, India, in 1991 and 1996, respectively, the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2006, and the D.Sc. (Habilitation) degree in control, informatics and electrical engineering from the Gdansk University of Technology, Poland, in 2019. He has been employed as a Lecturer with the Department of Electrical Engineering, AMU, since 1991, where he has served as a Full Professor until August 2016. He is currently a Full Professor with the Department of Electrical Engineering, Qatar University, Doha, Qatar, and a Former Full Professor of electrical engineering with AMU. He has published widely in international journals and conferences. His research findings related to power electronics, variable speed drives, and renewable energy sources. He has authored/coauthored more than 420 research articles and four books and several chapters in edited books. He has supervised several large research and development projects worth more than multimillion USD. He has supervised and co-supervised several Ph.D. students. His research interests include smart grid, complex energy transition, active distribution networks, electric vehicles drivetrain, sustainable development and energy security, distributed energy generation, and multiphase motor drive systems. He is also a Fellow IET, U.K., and IE, India. He received the Maulana Tufail Ahmad Gold Medal for his B.Sc. Engg. degree (electrical) from AMU in 1991. He was a recipient of Outstanding Faculty Merit Award academic year 2014–2015 and the research excellence awards 2015 and 2019 from Qatar University. He also received several best research papers awards, e.g., from IEEE ICIT-2013, IET-SEISCON-2013, SIGMA 2018, IEEE CENCON 2019, and IEEE ICIOT 2020. He is also the Vice-Chair of the IEEE Qatar Section. He is also an Associate Editor of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE ACCESS, the Editor-in-Chief of *i-manager's Journal of Electrical Engineering*, and a Former Associate Editor of IEEE TRANSACTIONS ON INDUSTRY APPLICATION.

MARIF DAULA SIDDIQUE (Member, IEEE) was born in Chhapra, India, in 1992. He received the B.Tech. and M.Tech. degrees in electrical engineering from Aligarh Muslim University (AMU), in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia. He is also working as a Research Assistant with the Department of Electrical Engineering, Qatar University, Doha, Qatar. He has authored or coauthored more than 30 publications in international journals and conference proceedings. He is serving as a regular reviewer for various journals of IEEE and IET. His research interests include step-up power electronics converters (dc/ac, and dc/dc), multilevel inverter topologies, and their control. He received the Best Research Paper Award from GUCON-2020.

JAGABAR SATHIK MOHAMED ALI (Senior Member, IEEE) was born in Thanjavur, India, in 1979. He received the B.E. degree in electronics and communication engineering from Madurai Kamarajar University, Madurai, India, in 2002, and the M.E. and Ph.D. degrees from the Faculty of Electrical Engineering, Anna University, Chennai, India, in 2004 and 2016, respectively. He is currently a Postdoctoral Fellow with the Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He is also an Associate professor with the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai, India. He is a consultant of various power electronics companies for the design of power electronics converters. He has authored more than 50 articles publications in international journals and conference proceedings. He is serving as a regular reviewer for several journals, including the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, *Transactions on Power Electronics*, *IET Power Electronics*, and IEEE ACCESS. His current research interests include multilevel inverters, grid-connected inverters, and power electronics converters and its applications to renewable energy systems.



SAAD MEKHILEF (Senior Member, IEEE) received the bachelor's degree in electrical engineering from the University of Setif, Setif, Algeria, in 1995, and the master's degree in engineering science and the Ph.D. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1998 and 2003, respectively. He is currently a Professor and the Director of the Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering, University of Malaya. He is also the Dean of the Faculty of Engineering, University of Malaya. He is also a Distinguished Adjunct Professor with the Faculty of Science, Engineering and Technology, School of Software and Electrical Engineering, Swinburne University of Technology, Melbourne, VIC, Australia. He has authored or coauthored more than 550 publications in international journals and conference proceedings. His current research interests include power converter topologies, control of power converters, renewable energy, and energy efficiency. He is serving as an Editor for *Renewable & Sustainable Energy Reviews* and an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE OPEN JOURNAL OF INDUSTRIAL ELECTRONICS, *International Journal of Circuit Theory and Applications*, and *Journal of Power Electronics*. He is also serving as a Guest Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS, *IET Power Electronics*, *IET Renewable Power Generation*, and *International Transactions on Electrical Energy Systems*.

JOHN LAM (Senior Member, IEEE) received the master's and Ph.D. degrees in electrical engineering from Queen's University, Kingston, ON, Canada, in 2006 and 2010, respectively.

He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, Lassonde School of Engineering, York University, Toronto, ON, Canada. He is also the Director of the Advanced Power Electronics Laboratory for Sustainable Energy Research at York. His research interests include power electronic converters with soft-switching techniques, wide bandgap-based power conversion systems, energy storage, and renewable energy application. He received several awards, including the Outstanding Reviewer Award from the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2018, the Star Reviewer Award from the IEEE JOURNAL AND EMERGING SELECTED TOPICS ON POWER ELECTRONICS in 2019, and the Lassonde Innovation Award Early Researcher from York University in 2020. He is also an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.